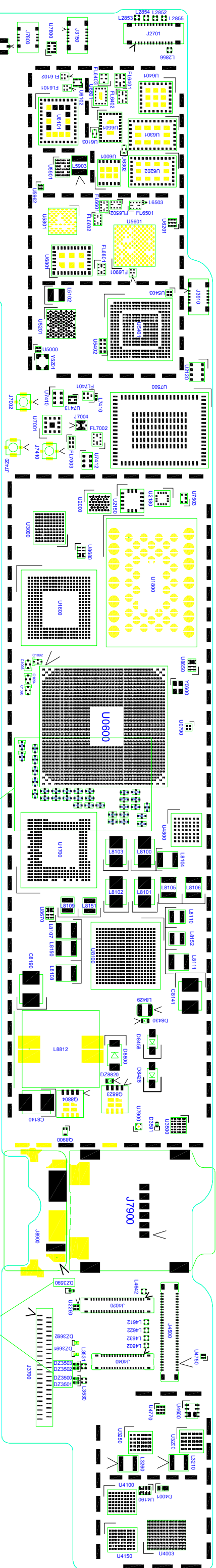


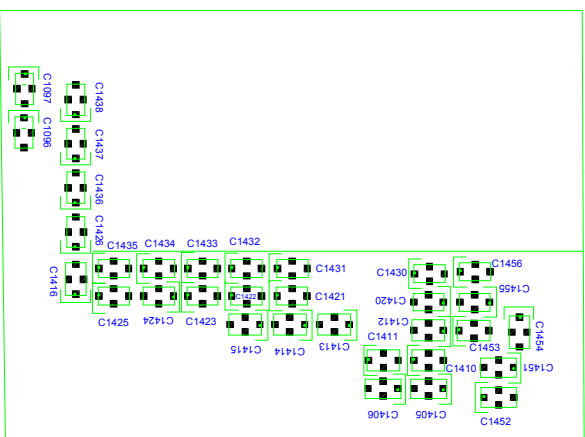
VIETMOBILE.VN

IPAD AIR 2

SCHEMATIC DIAGRAM



備註: "DZ3500,DZ3501,DZ3502,DZ3503,DZ3590"
以上位置使用337S0104,377S0155為有極性;使用377S0184
則無極性!



RL EVT MLB B 820-3633-05 TOP 面極性圖 20140503

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

MLB B - PVT

LAST_MODIFIED=Mon Sep 29 18:09:18 2014

RADIO_MLB SYNC VER 0.109.0

WIFI_DEV SYNC VER 0.68.0

ROTTERDAM SYNC VER 0.11.0

REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

B

0003279770

PRODUCTION RELEASED

2014-09-29

PDF

CSA

CONTENTS

SYNC MASTER

DATE

1

1

TABLE OF CONTENTS

N/A

N/A

2

2

BLOCK DIAGRAM: SYSTEM

N/A

N/A

3

4

BOM TABLES

N/A

N/A

4

5

SOC: MISC & ALIASES

N/A

N/A

5

6

SOC: MAIN

N/A

N/A

6

7

SOC: I/OS

N/A

N/A

7

8

SOC: NAND

N/A

N/A

8

9

SOC: MIPI, ISP

N/A

N/A

9

10

SOC: EDP, PCIE

N/A

N/A

10

11

SOC: DDR

N/A

N/A

11

12

SOC: IO POWER

N/A

N/A

12

13

SOC: SOC POWER AND GND

N/A

N/A

13

14

SOC: CPU, GPU, SRAM POWER

N/A

N/A

14

16

DDR: CHANNEL 0 AND 1

N/A

N/A

15

17

DDR: CHANNEL 2 AND 3

N/A

N/A

16

18

NAND

N/A

N/A

17

20

SENSOR: OSCAR

N/A

N/A

18

21

SENSOR: CARBON, PHOS+, MAGN

N/A

N/A

19

22

SENSOR: HALL EFFECT

N/A

N/A

20

27

CAMERA: CAM CONNS

N/A

N/A

21

28

CAMERA: CAM SUPPORT

N/A

N/A

22

30

AUDIO: L81 CODEC

N/A

N/A

23

31

AUDIO: HP/DMIC FLEX CONNS

N/A

N/A

24

32

AUDIO: SPEAKER AMPS

N/A

N/A

25

35

IO: TRISTAR

N/A

N/A

PDF

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SYNC MASTER

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IO: FILTERS

N/A

N/A

27

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IO: HOTBAR PADS

N/C

N/A

28

39

IO: BUTTON FLEX CONN

N/A

N/A

29

40

GRAPE: STINGER & CONN

N/A

N/A

30

41

GRAPE: CUMULUS

N/A

N/A

31

45

DISPLAY: CONNECTOR

N/A

N/A

32

46

DISPLAY: EDP SUPPORT

N/A

N/A

33

47

MESA: SUPPORT

N/A

N/A

34

48

ROTTERDAM

ROTTERDAM

05/13/2014

35

50

CELL: PROBE PTS & DEBUG CONN

RADIO

09/29/2014

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51

CELL: BB PMU (1/2)

RADIO

09/29/2014

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52

CELL: BB PMU (2/2)

RADIO

09/29/2014

38

53

CELL: BASEBAND (1/2)

RADIO

09/29/2014

39

54

CELL: BASEBAND (2/2)

RADIO

09/29/2014

40

55

CELL: BASEBAND (3/3)

RADIO

09/29/2014

41

56

CELL: RF TXCVR (1/3)

RADIO

09/29/2014

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57

CELL: RF TXCVR (2/3)

RADIO

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58

CELL: RF TXCVR (3/3)

RADIO

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CELL: QFE DCDC

RADIO

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CELL: 2G PA

RADIO

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CELL: VLB PAD

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CELL: LB PAD

RADIO

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CELL: MB PAD

RADIO

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CELL: RX DIV (2/2)

RADIO

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CELL: GPS

RADIO

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CELL: ANT FEEDS & GPS (J82)

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WIFI/BT: J82 ANT INTERFACE

WIFI

09/29/2014

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WIFI/BT: WIFI/BT MODULE

WIFI

09/29/2014

58

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SENSOR: HAMMERHEAD

N/A

N/A

59

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CELL: SIM AND ANT SW FILT

N/A

N/A

60

81

PMU: ARABELA (1/3)

N/A

N/A

61

82

PMU: ARABELA (2/3)

N/A

N/A

62

83

PMU: ARABELA (3/3)

N/A

N/A

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84

POWER: J82 SPECIFIC

N/A

N/A

64

86

POWER: EXTERNAL SWITCHES

N/A

N/A

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88

PMU: CHARGER BUCK

N/A

N/A

66

89

POWER: BATTERY CONN

N/A

N/A

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SOC: DEBUG

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ALIASES: BB/WLAN/BT

N/A

N/A

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TEST: TPS/HOLES/FIDUCUALS

N/A

N/A

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TEST: EE TP/PP

N/A

N/A

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TEST: CELL EE TP/PP

N/A

N/A

72

121

POWER: ALIASES

N/A

N/A

73

155

BB/WLAN VOLTAGE ATTRIBUTES

N/A

N/A

DRAWING

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0301	1	SCH,MLB-B,J82	SCH1	CRITICAL	
820-3633	1	PCBF,MLB-B,J82	PCB1	CRITICAL	

SCHEM,MLB-B,X190

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051-0301

REVISION

B.0.0

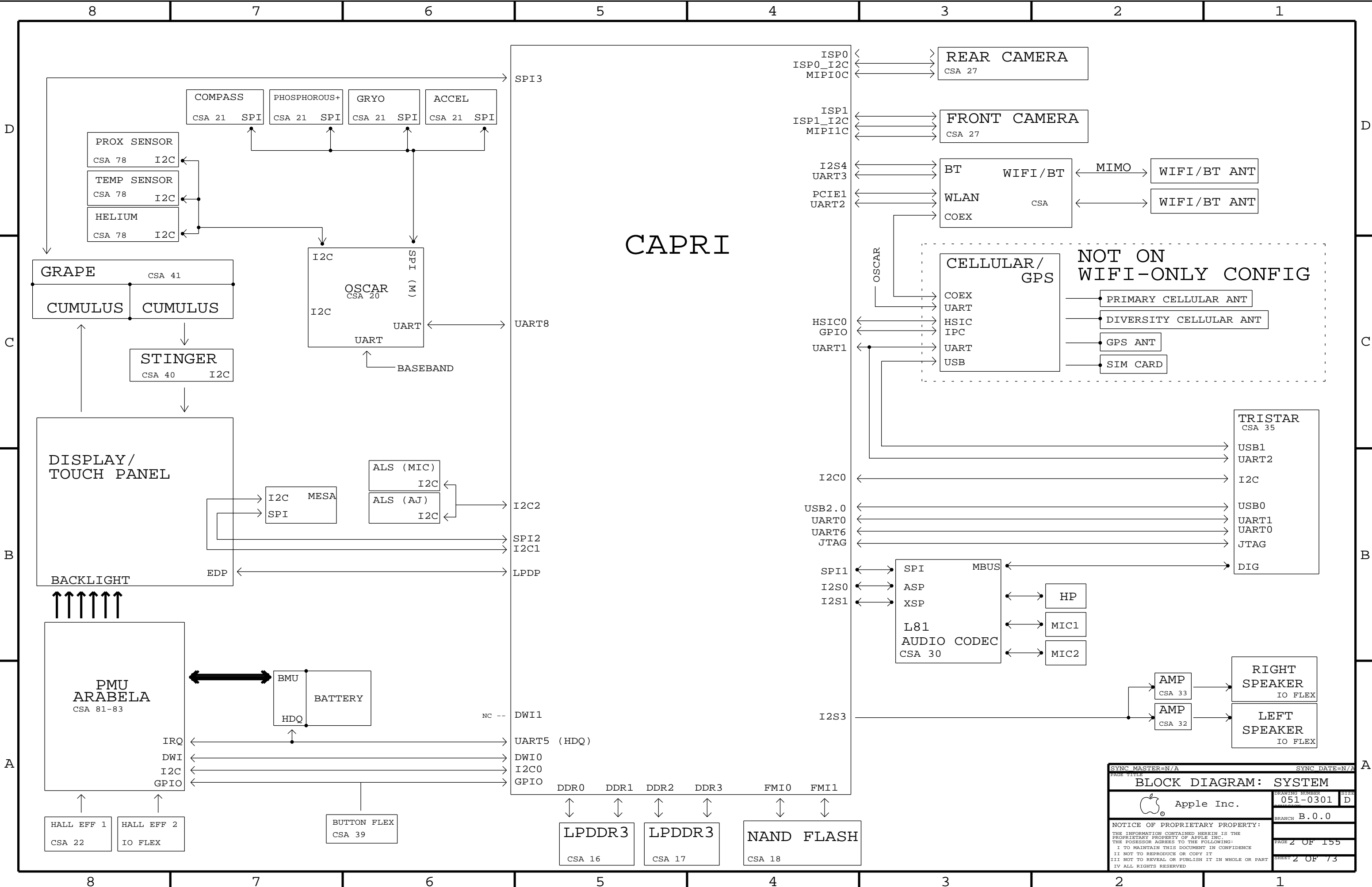
BRANCH

PAGE

1 OF 155

SHEET

1 OF 73



Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00016	1	IC,CAPRI,A1,PROD,ASE	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S00021	343S00016		U0600	IC,CAPRI,A1,PROD,SCK

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0675	1	IC, MPU, ARABEIA, D2297A0, TOP-AC, FCBG0A380	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0803	2	IC,CAPRI,DRAM,10X10MM,FBGA261	U1600,U1700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0804	333S0803		U1600,U1700	ELPIDA DRAM
333S00014	333S0803		U1600,U1700	SAMSUNG DRAM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0972	1	TOSHIBA 16GB MLC LYNM PPN1.5	U1800	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S1035	335S0972	16GB_PROD	U1800	HYNIX 16GB MLC 1YNM PPN1.5

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00011	1	SANDISK 64GB TLC 1YNM PPN1.5	U1800	CRITICAL	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00017	335S00011	64GB_PROD	U1800	TOSHIBA 64GB TLC 1Y3M PPN

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00012	1	SANDISK 128GB TLC 1YNM PPN1.5	U1800	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00018	335S00012	128GB_PROD	U1800	TOSHIBA 128GB TLC 19MM PPM

MECHANICAL PARTS


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-7118	1	RADIO FENCE X190	PD_FENCE_RADIO	CRITICAL	MLB_B
806-00001	1	AP FENCE X190	PD_FENCE_AP	CRITICAL	
806-6353	1	GRAPE FENCE X190	PD_FENCE_GRAPE	CRITICAL	

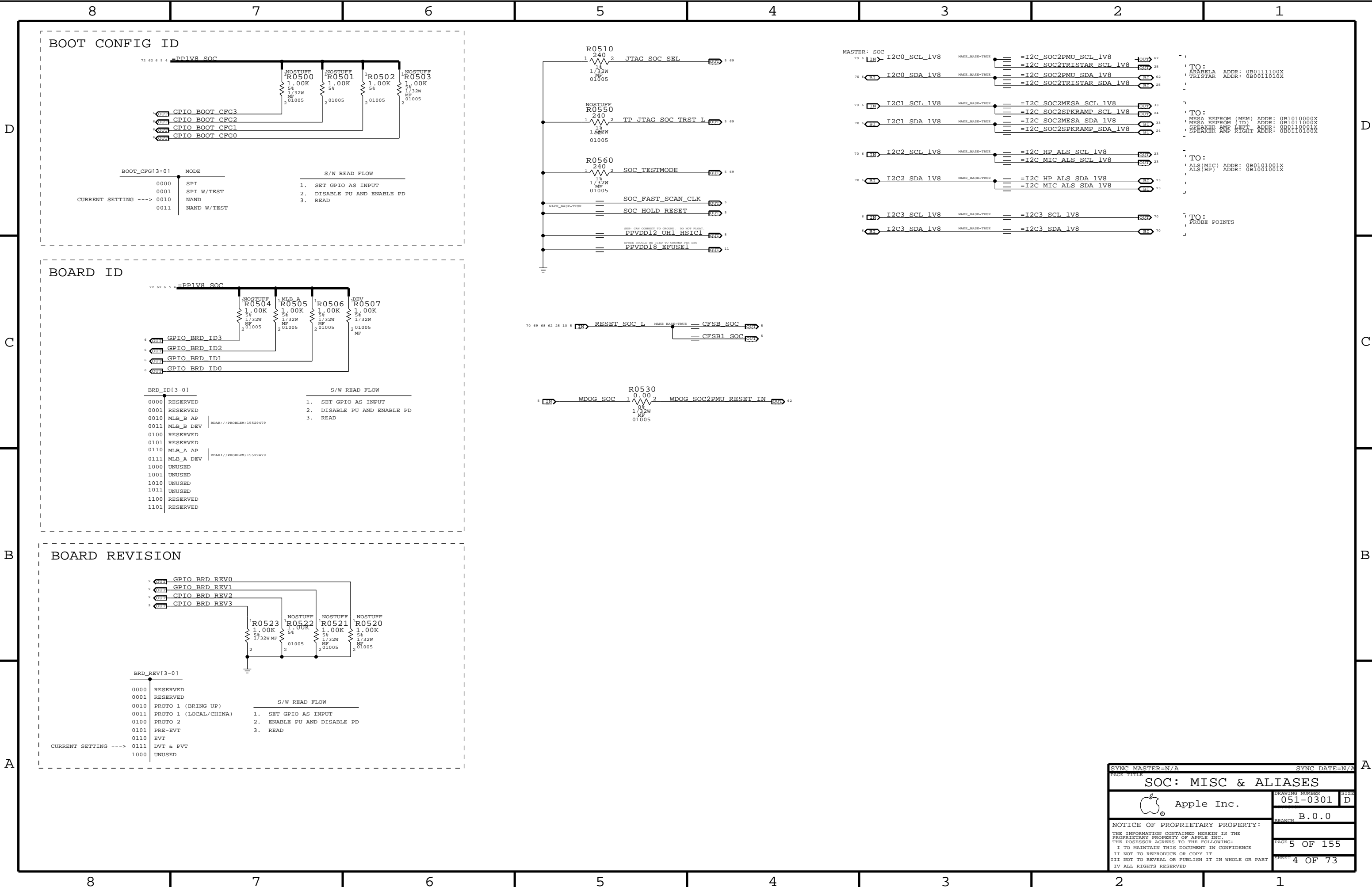
BARCODE LABEL/EEEE CODES

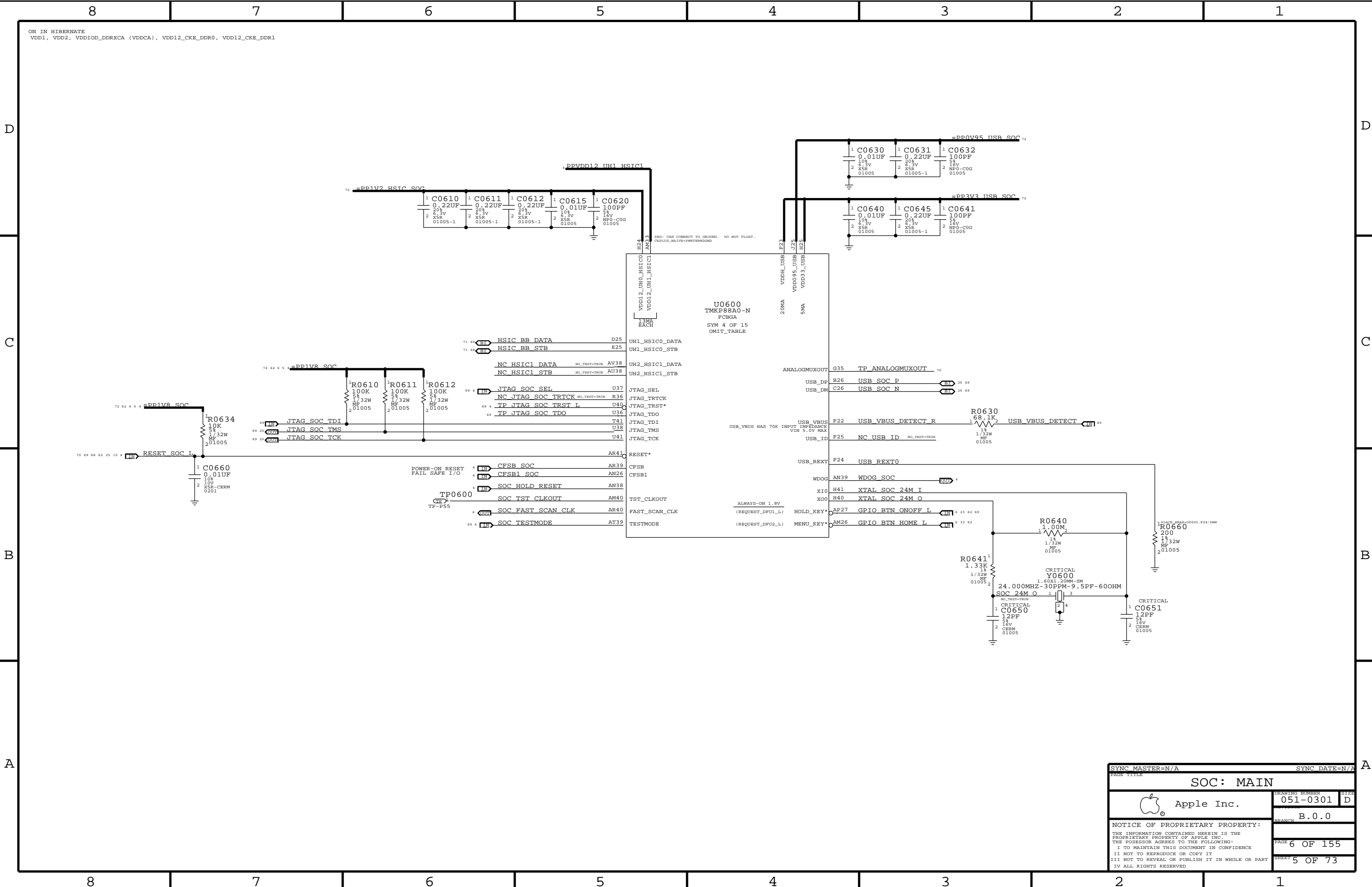
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-00067	1	EEEE FOR 639-5813 (MLB A 16GB)	EEEE_FQJ3	CRITICAL	EEEE_MLB_A_16GB
825-00067	1	EEEE FOR 639-5814 (MLB A 32GB)	EEEE_FQJ0	CRITICAL	EEEE_MLB_A_32GB
825-00067	1	EEEE FOR 639-5815 (MLB A 64GB)	EEEE_FQJ1	CRITICAL	EEEE_MLB_A_64GB
825-00067	1	EEEE FOR 639-5816 (MLB A 128GB)	EEEE_FQJ2	CRITICAL	EEEE_MLB_A_128GB
825-00067	1	EEEE FOR 639-4747 (MLB B 16GB)	EEEE_FH54	CRITICAL	EEEE_MLB_B_16GB
825-00067	1	EEEE FOR 639-5809 (MLB B 32GB)	EEEE_FQHY	CRITICAL	EEEE_MLB_B_32GB
825-00067	1	EEEE FOR 639-5810 (MLB B 64GB)	EEEE_FQHW	CRITICAL	EEEE_MLB_B_64GB
825-00067	1	EEEE FOR 639-5811 (MLB B 128GB)	EEEE_FQHV	CRITICAL	EEEE_MLB_B_128GB

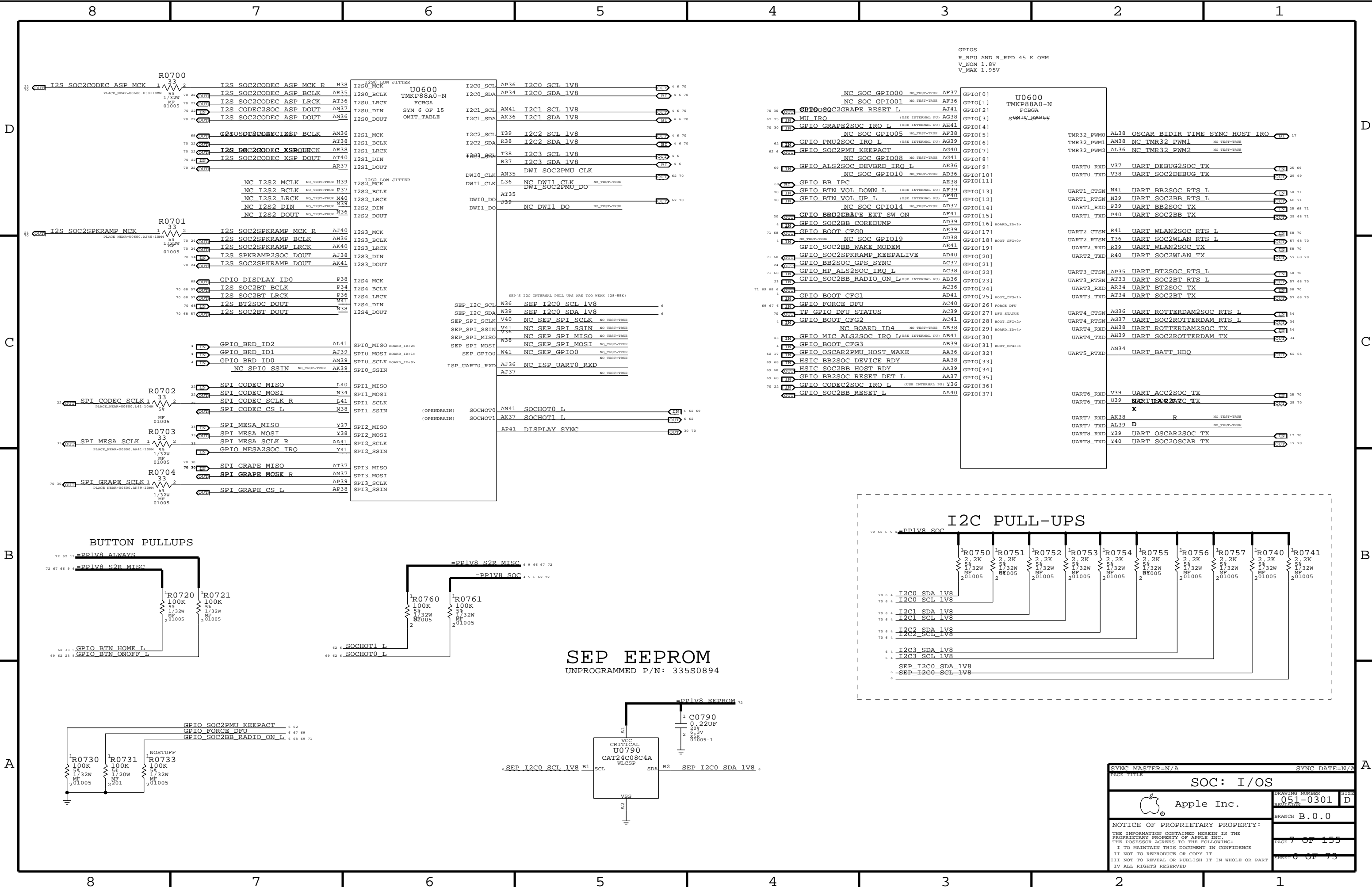
CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

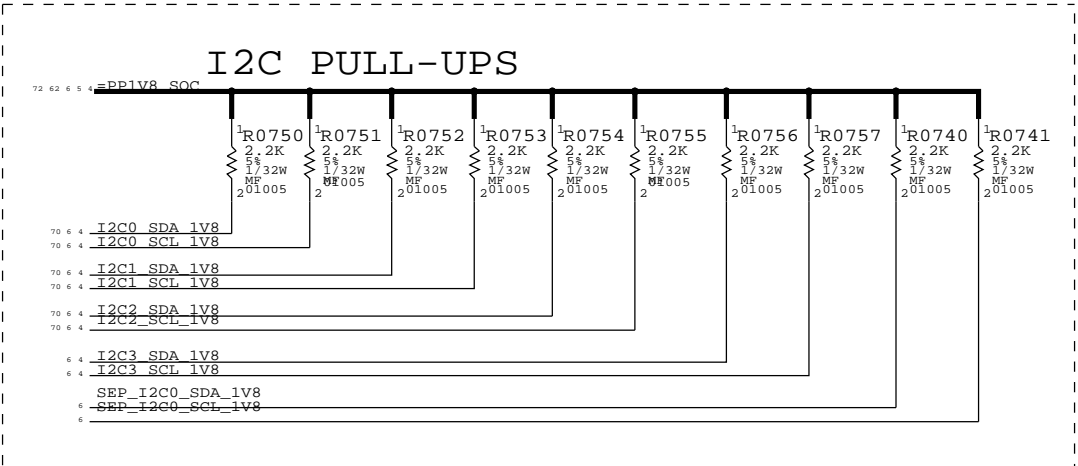
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BOM TABLES			
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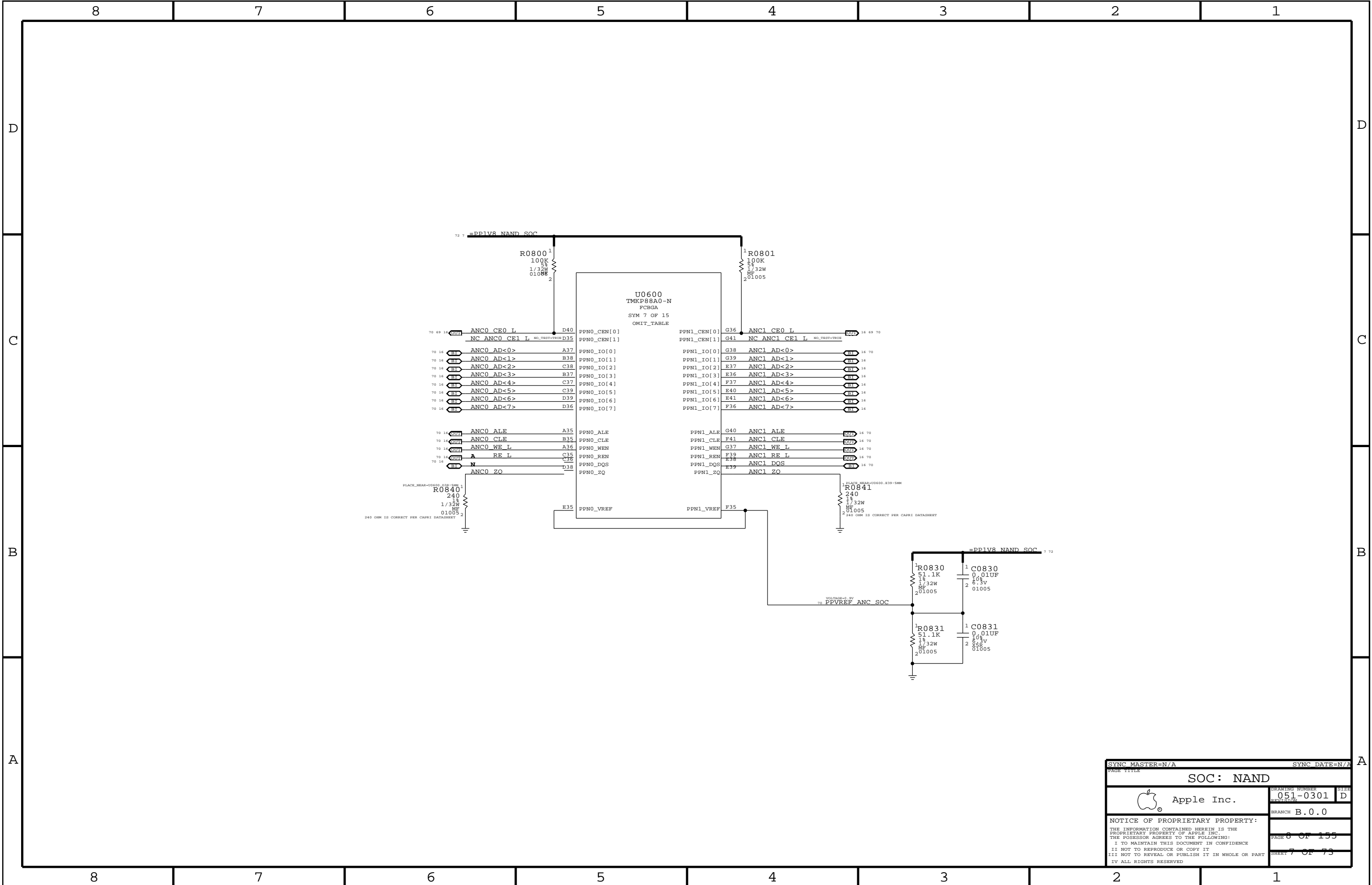


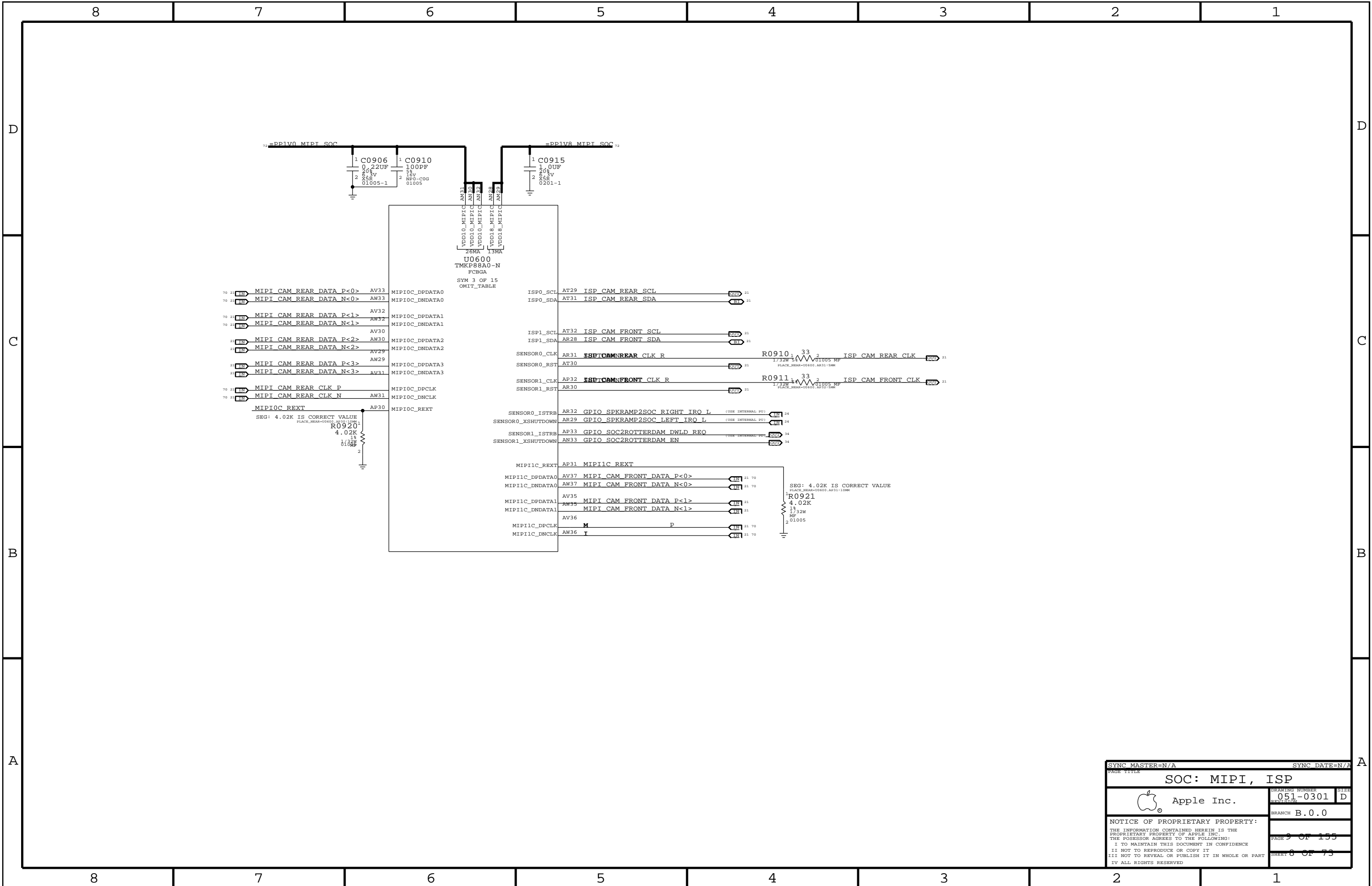


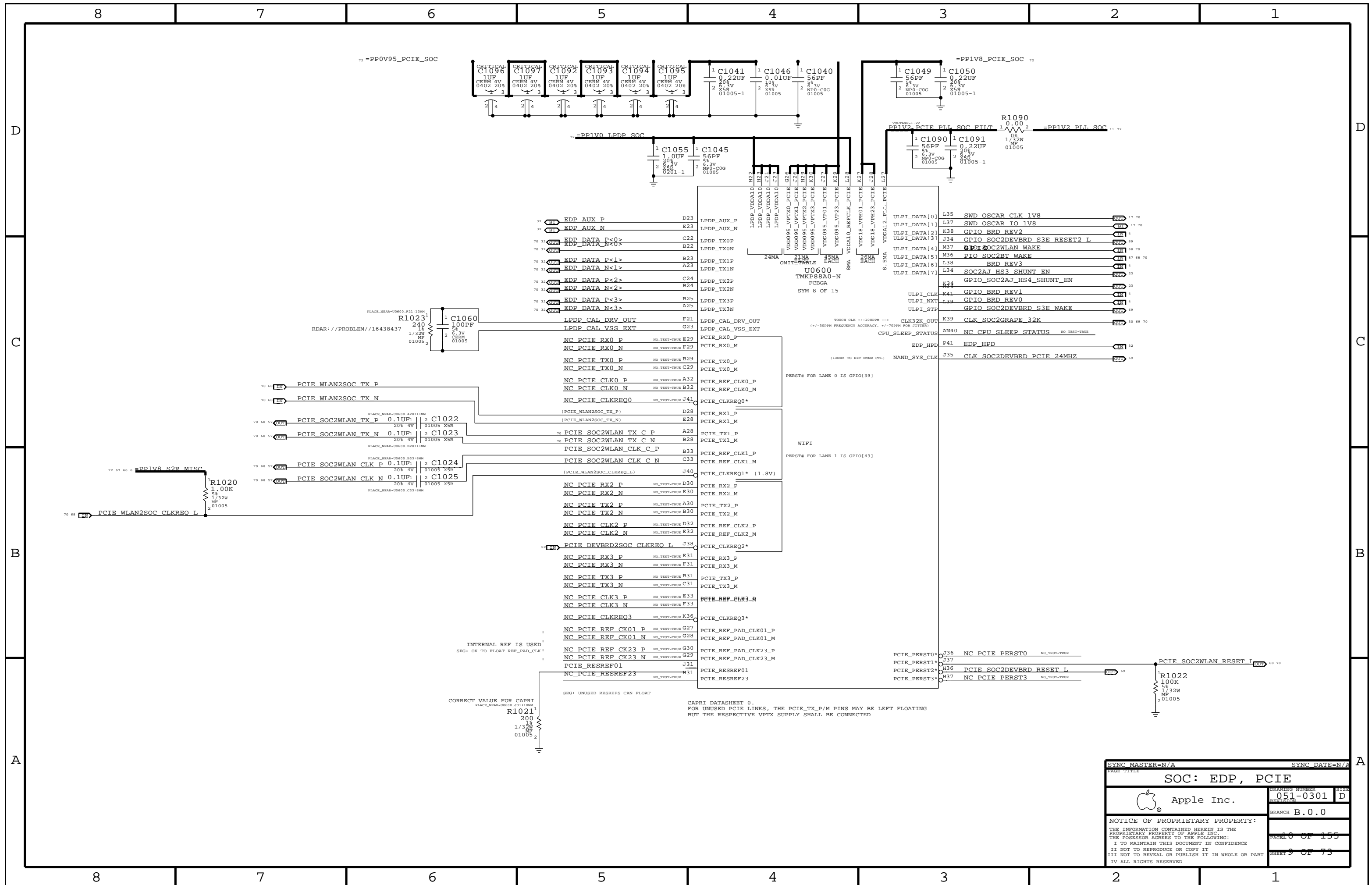
SEP EEPROM
UNPROGRAMMED P/N: 335S0894

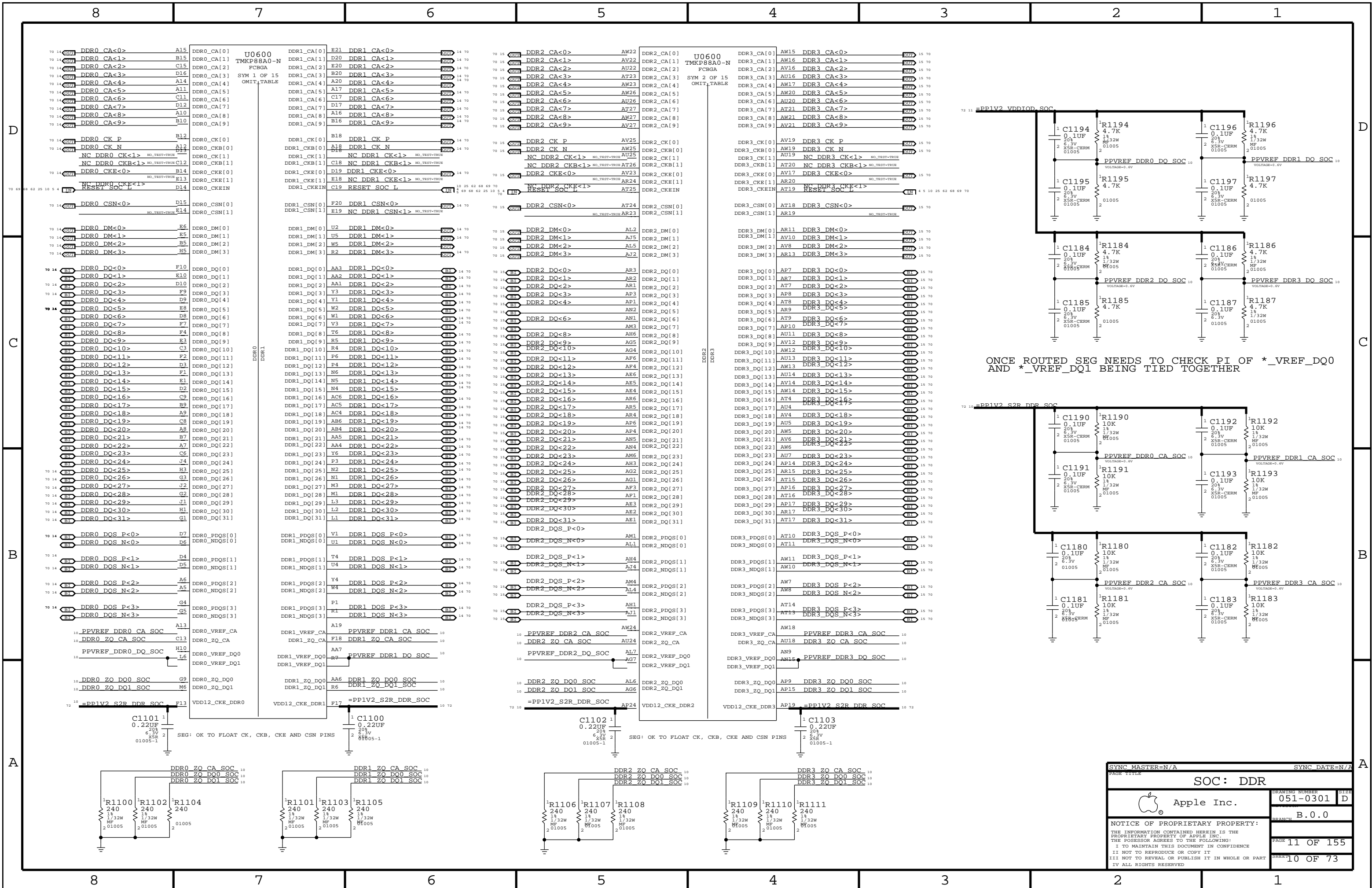


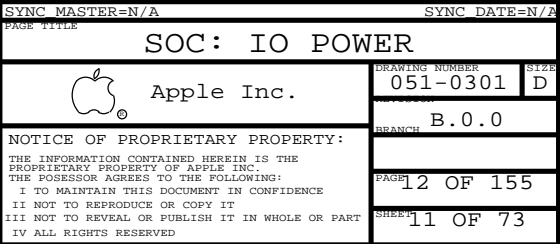
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Drawing NUMBER		SIZE	
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BRANCH		B.0.0	
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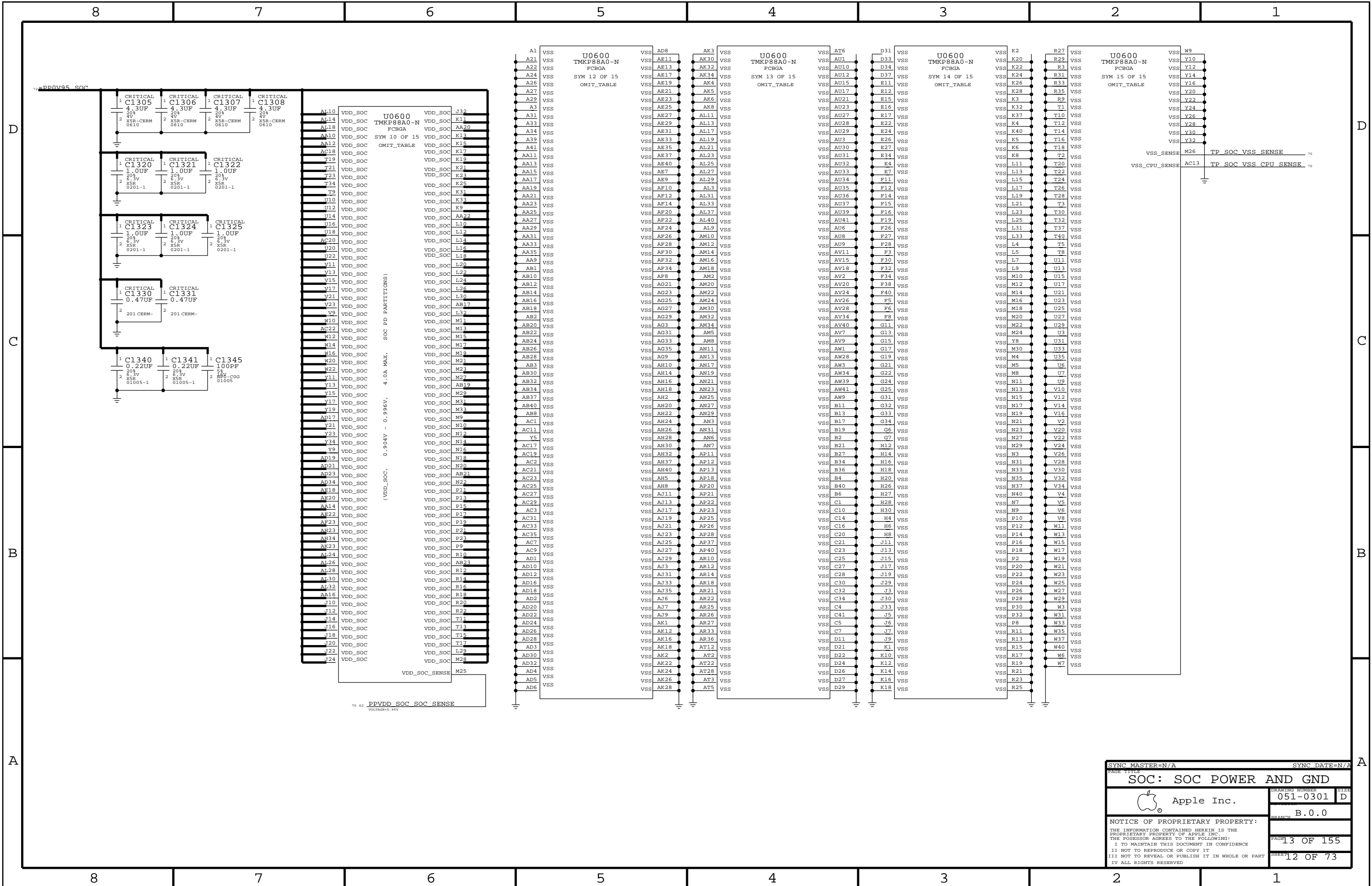


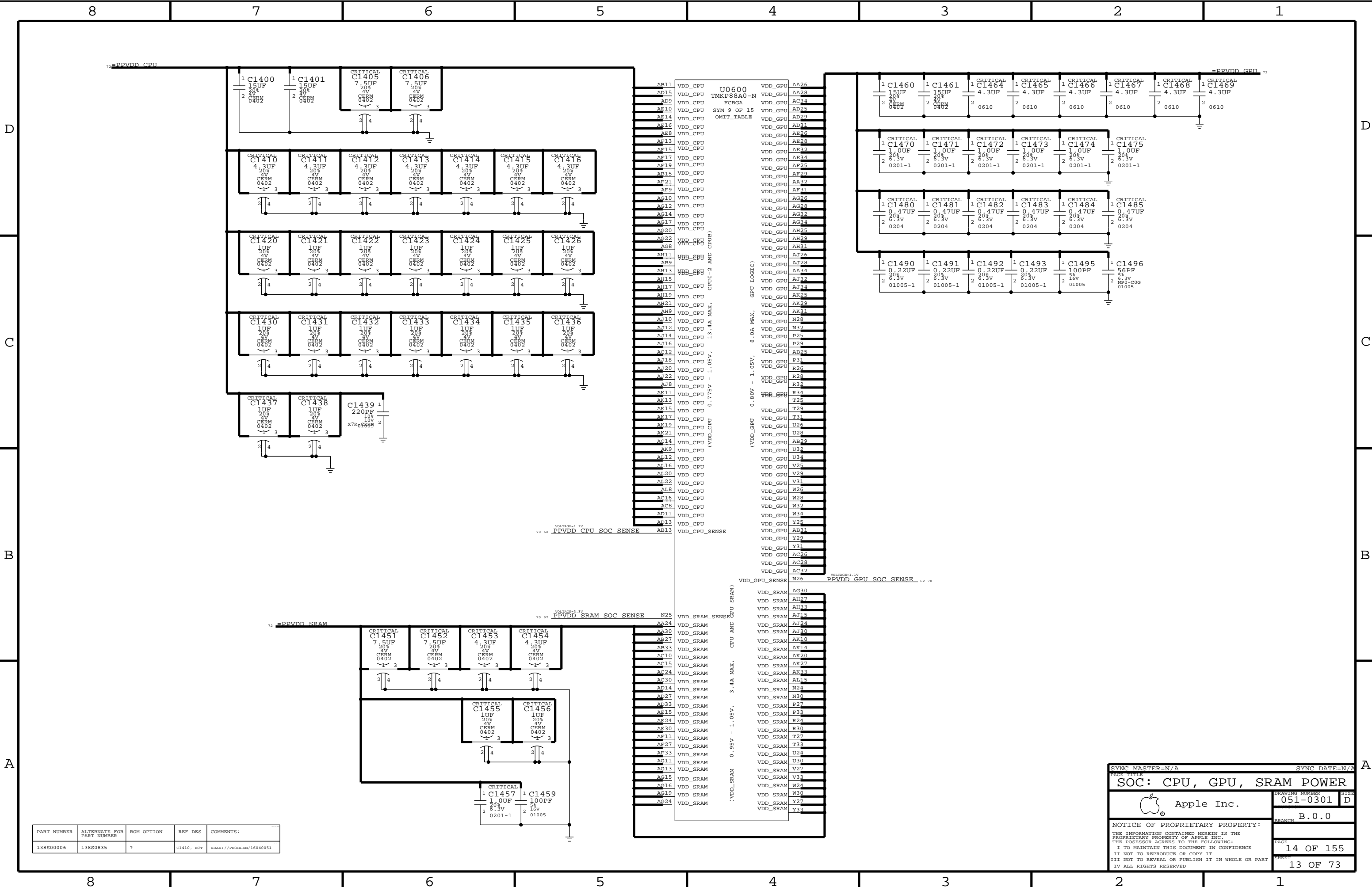






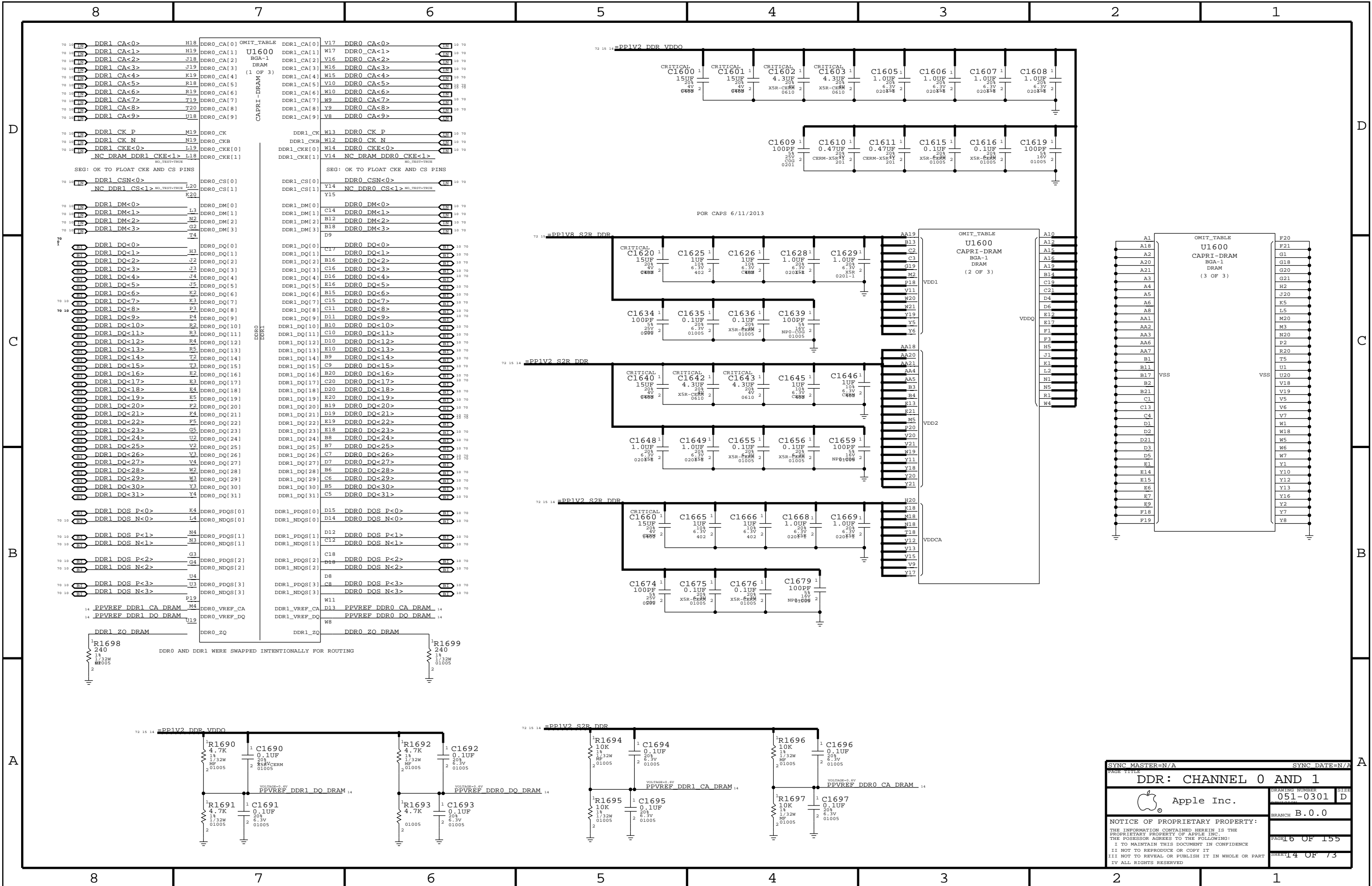


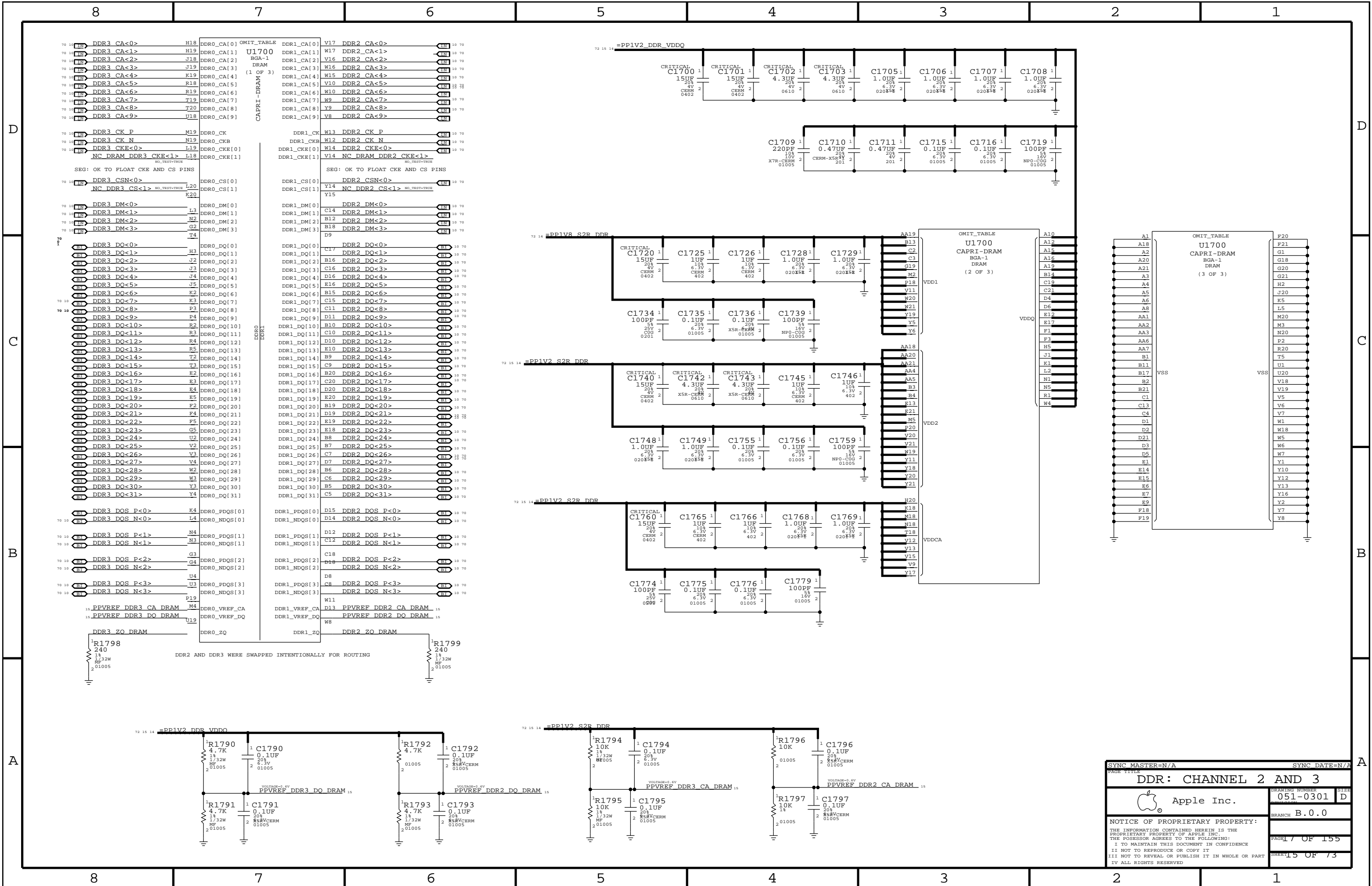


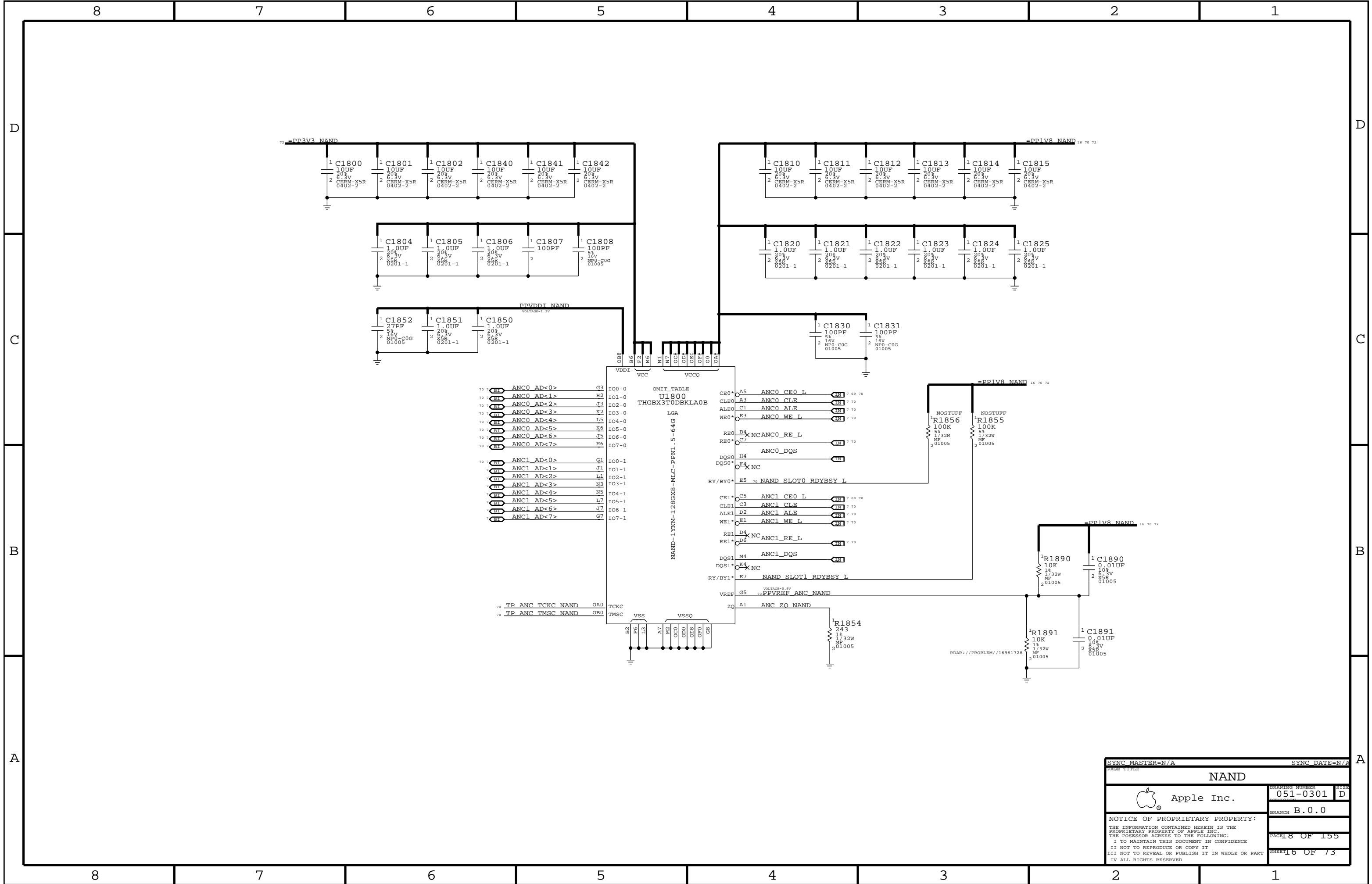


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138S00006	138S0835	?	C1410, KCT	RDAR:///PROBLEM/16040051

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SOC: CPU, GPU, SRAM POWER		051-0301		D	
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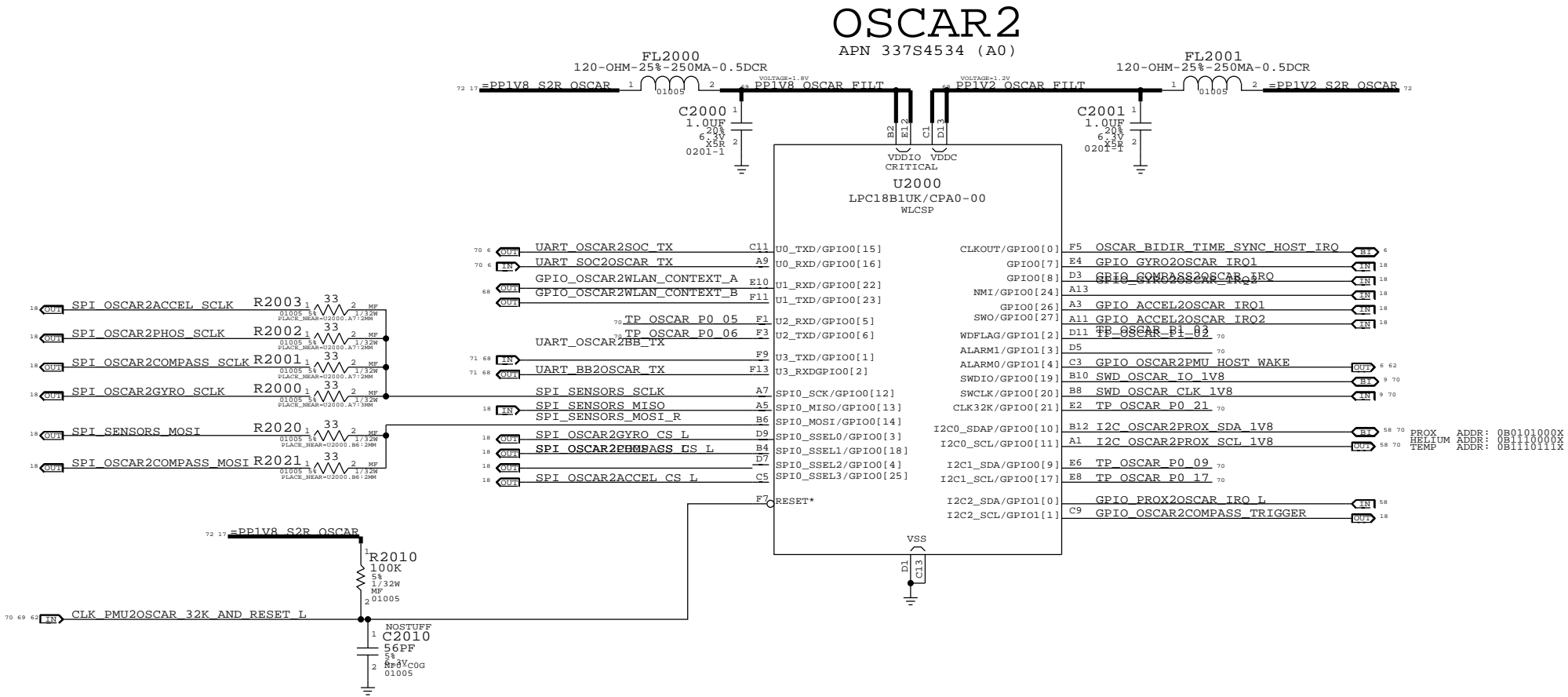






OSCAR

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155S00016	155S0686		FL2000 & MORE	RDAR://PROBLEM/15809407



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B

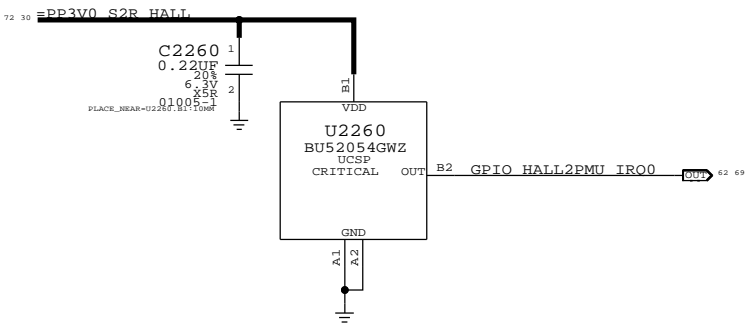



A

A

HALL EFFECT

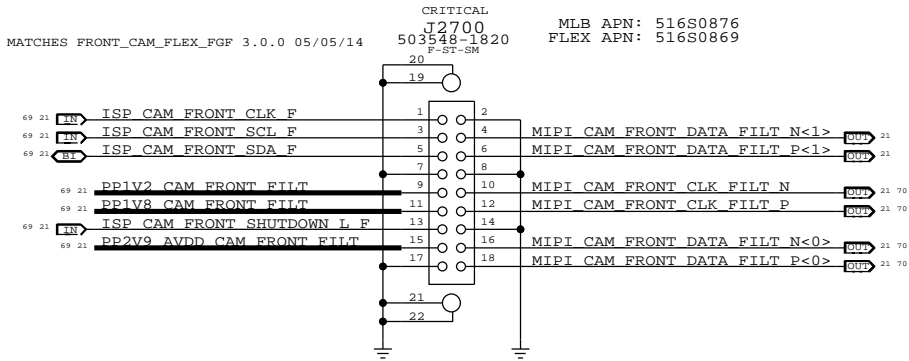
HALL EFFECT
APN 353S3687



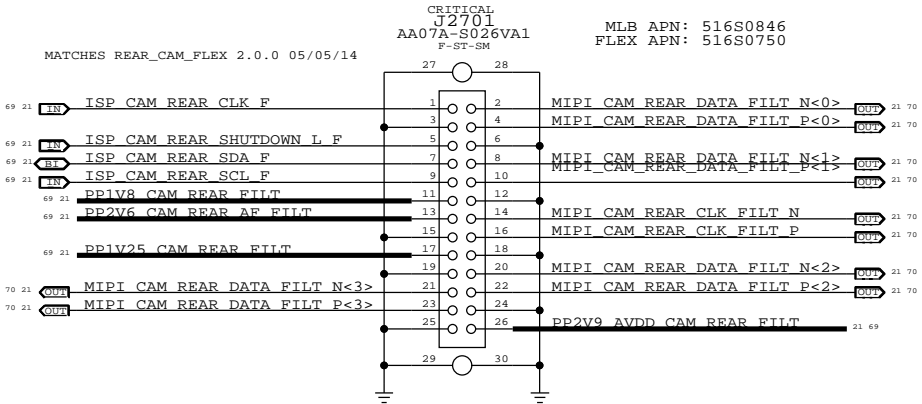
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		PAGE	22 OF 155
		SHEET	19 OF 73


FRONT & REAR CAMERA CONNECTORS

FRONT CAMERA CONNECTOR

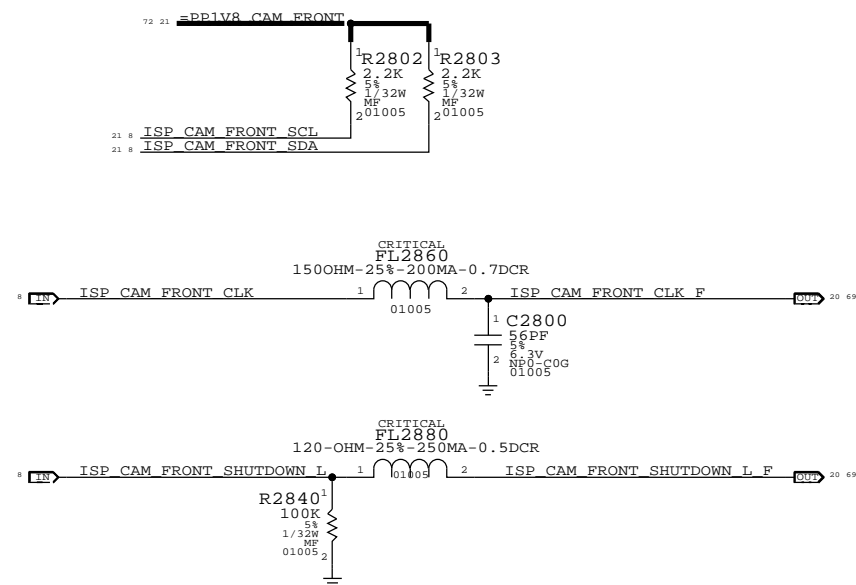
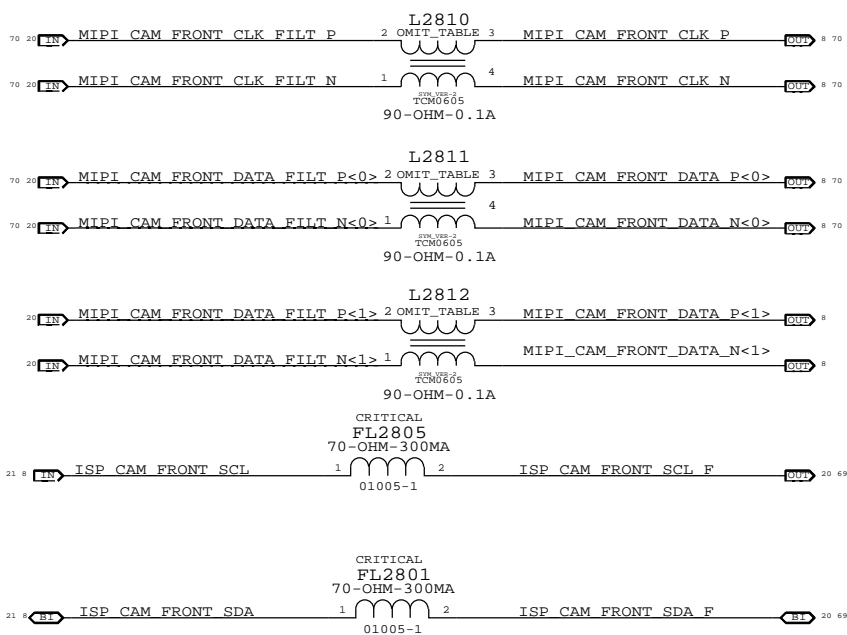
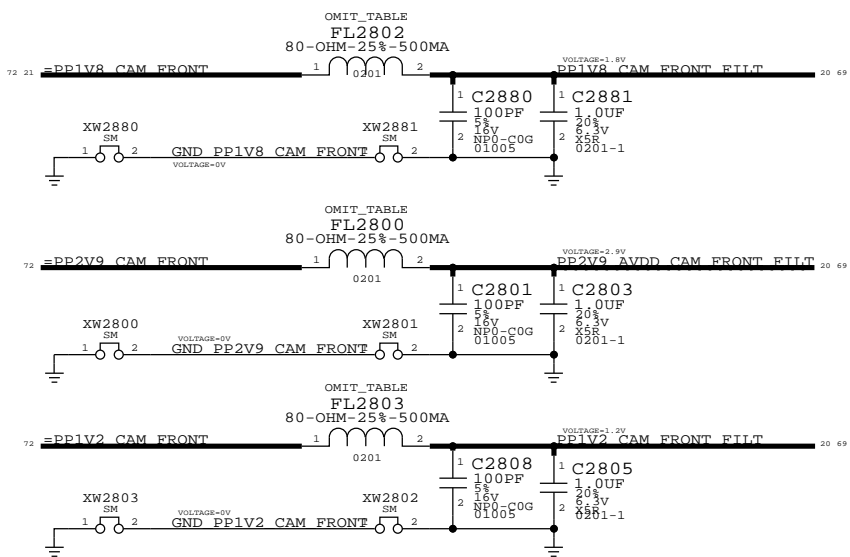


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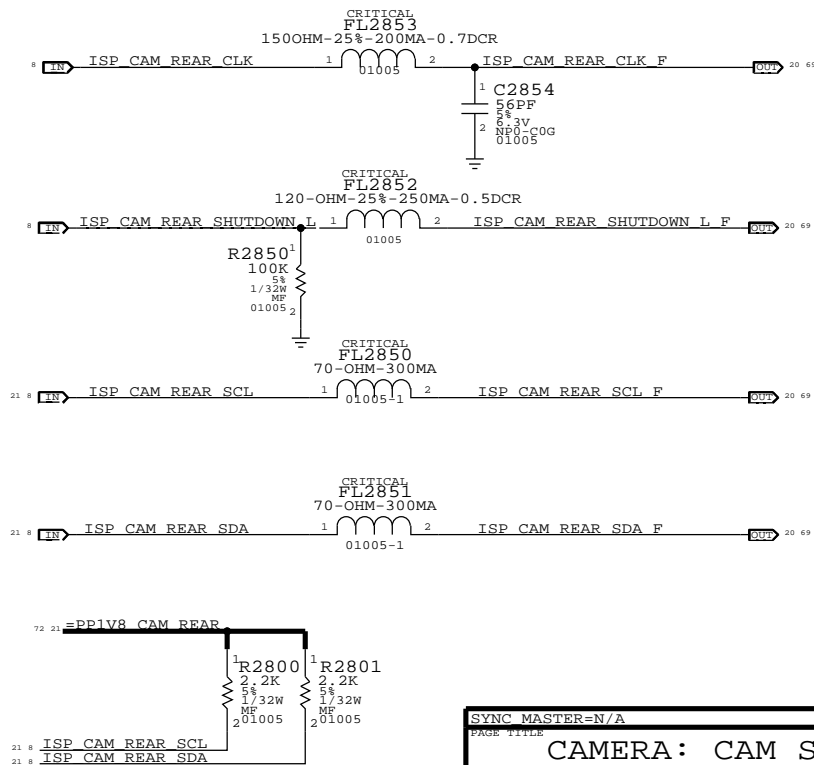
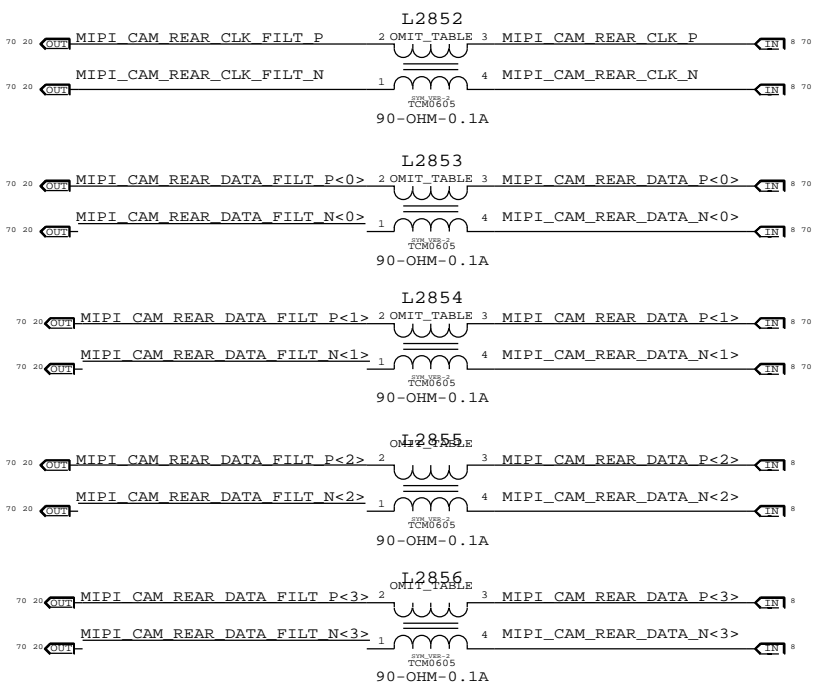
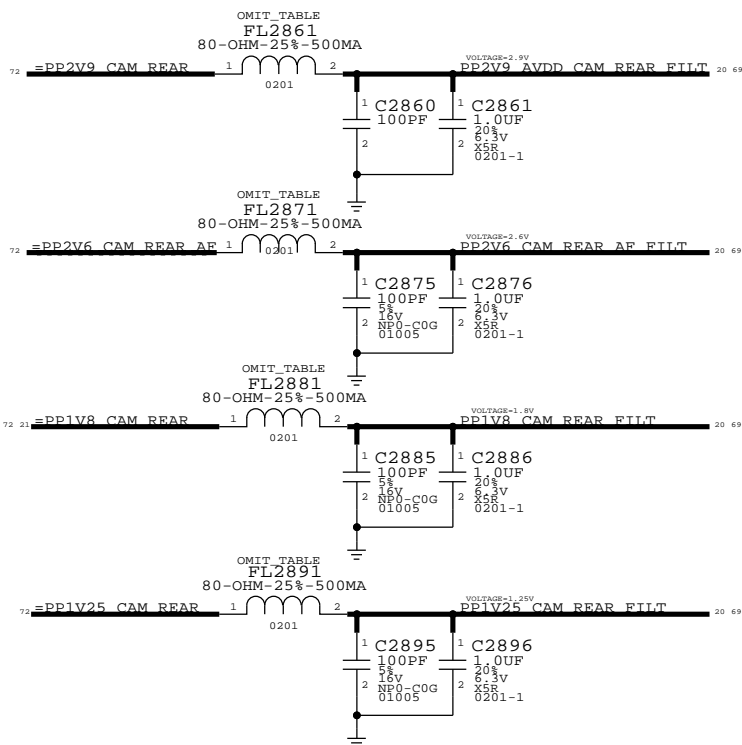



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PAGE TITLE			
CAMERA: CAM CONNS			
 Apple Inc.		DRAWING NUMBER	81428
		051-0301	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	B.0.0
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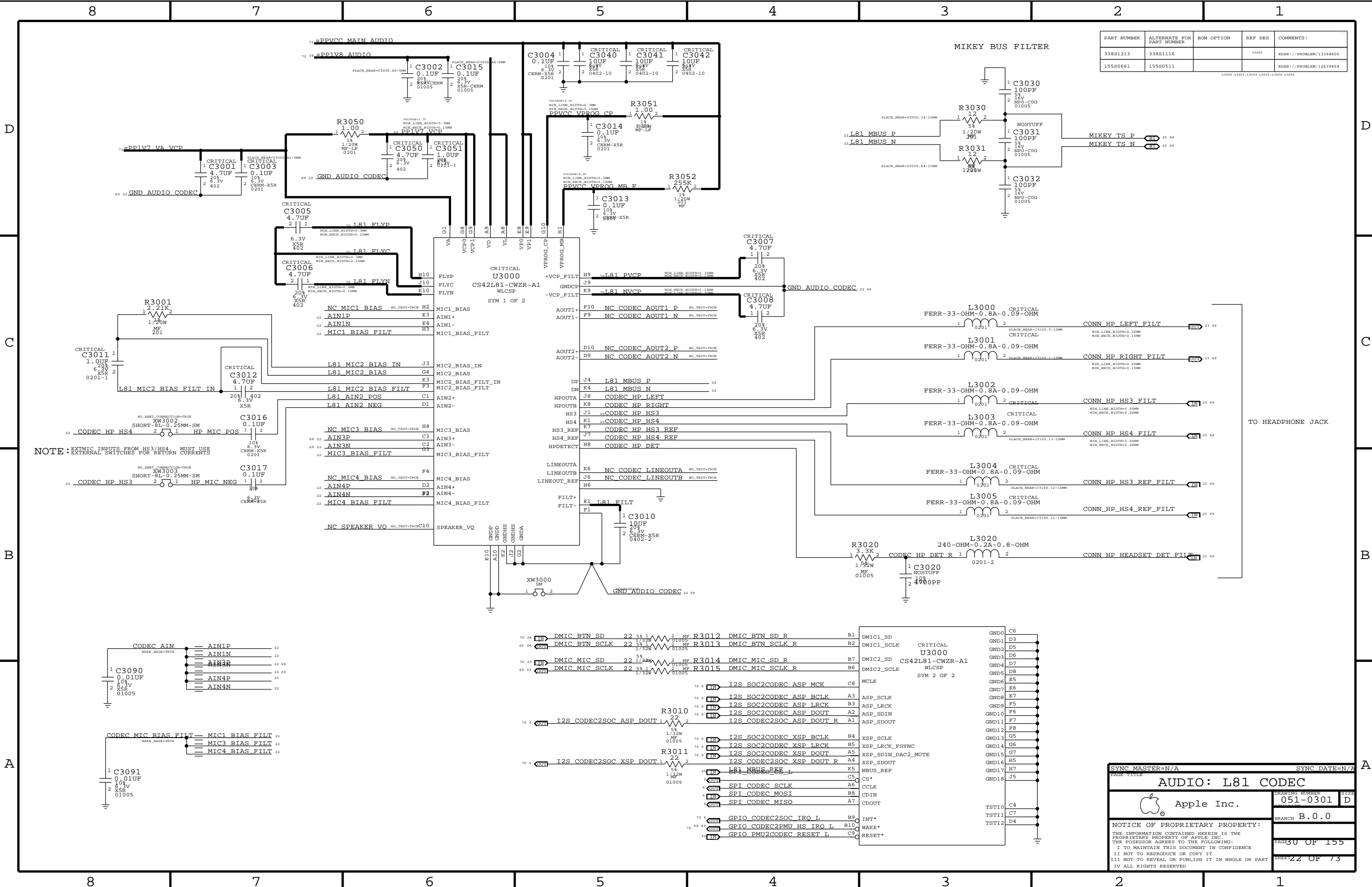
FRONT CAMERA SUPPORT



REAR CAMERA SUPPORT

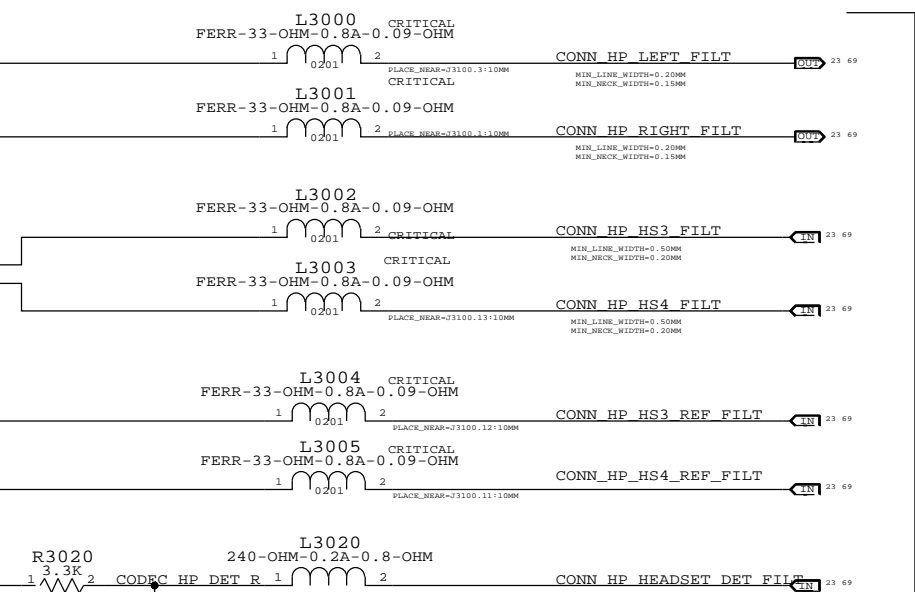
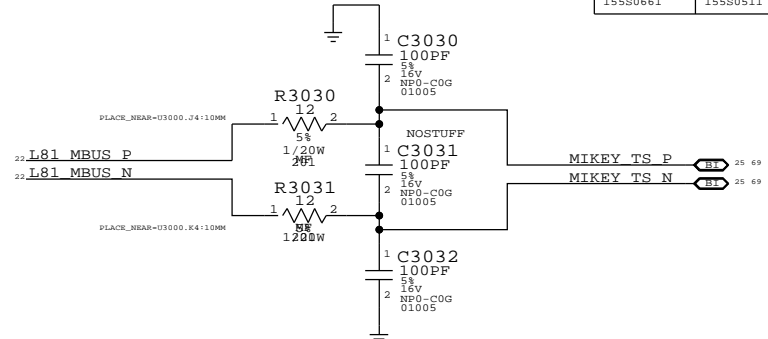


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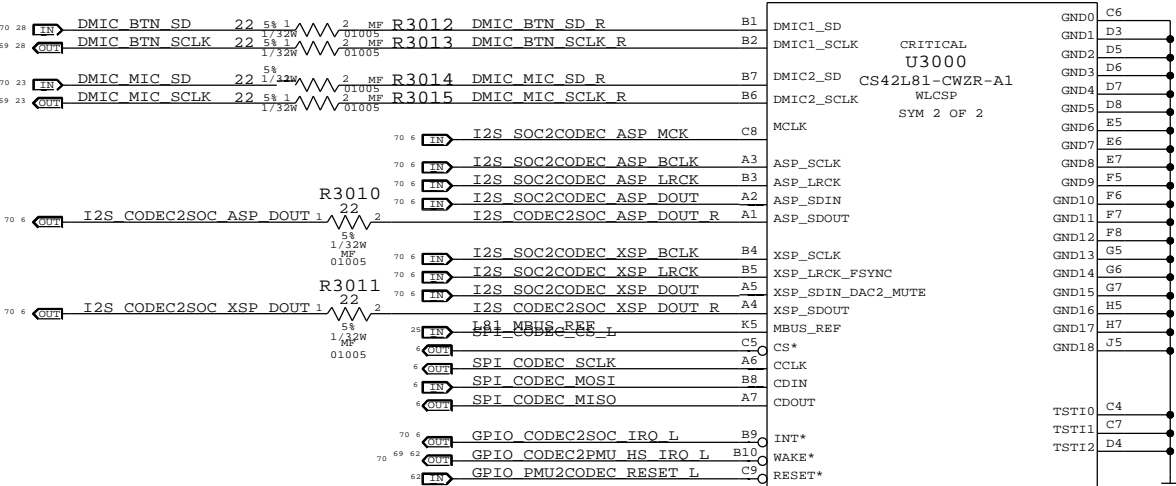
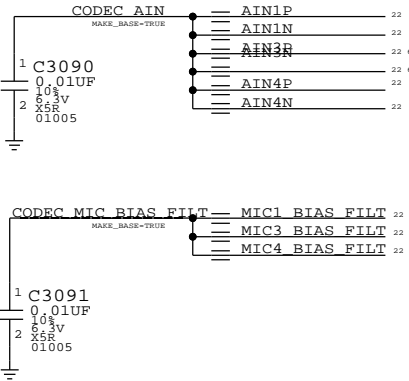
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155S0661	155S0511			RDAR:///PROBLEM/12639854

MIKEY BUS FILTER



TO HEADPHONE JACK

NOTE: EXTMIC INPUTS FROM HS3/HS4. MUST USE EXTERNAL SWITCHES FOR RETURN CURRENTS



SYNC MASTER=N/A

SYNC DATE=N/A

AUDIO: L81 CODEC

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PAGE

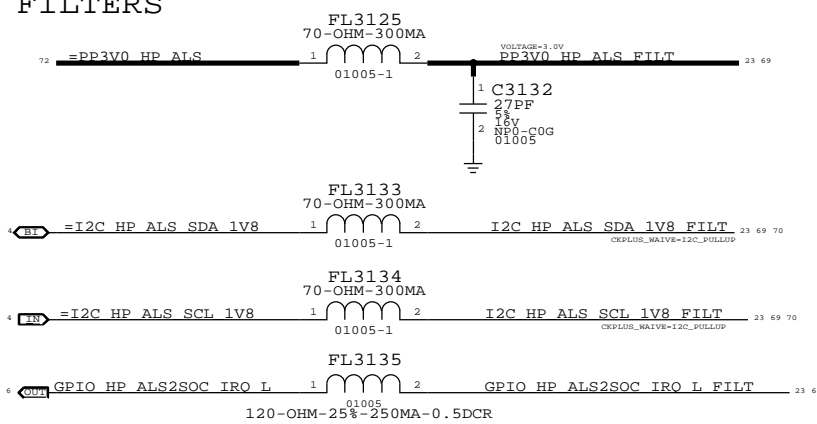
30 OF 155

SHEET

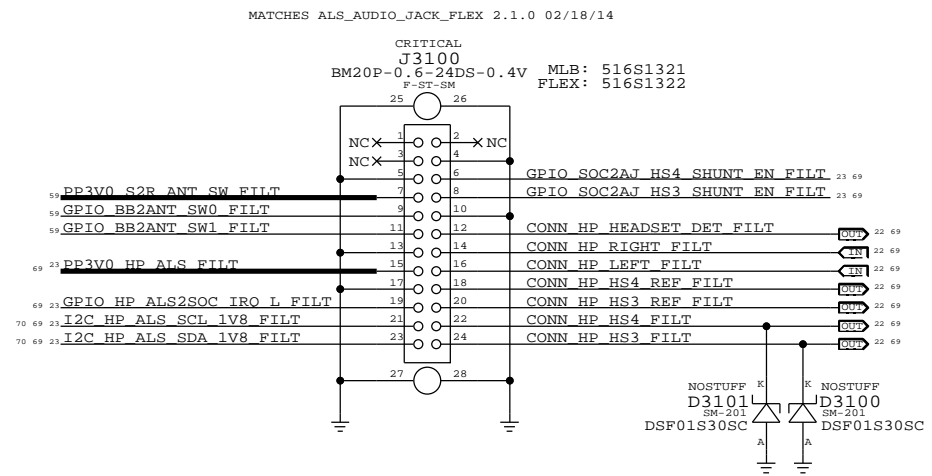
22 OF 73

AUDIO JACK AND DMIC CONNN

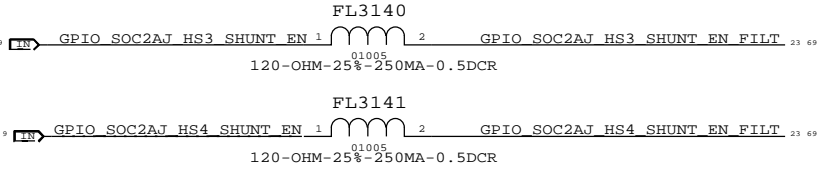
ALS FILTERS



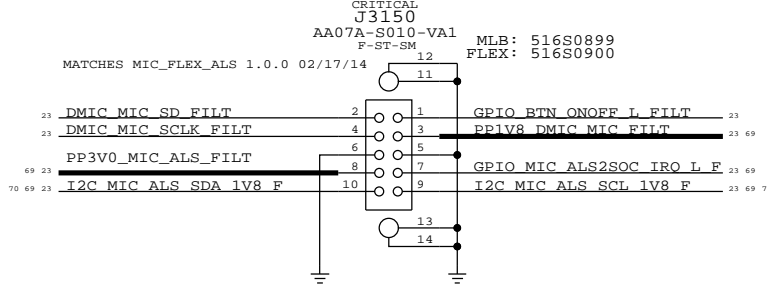
AUDIO JACK B2B CONNECTOR



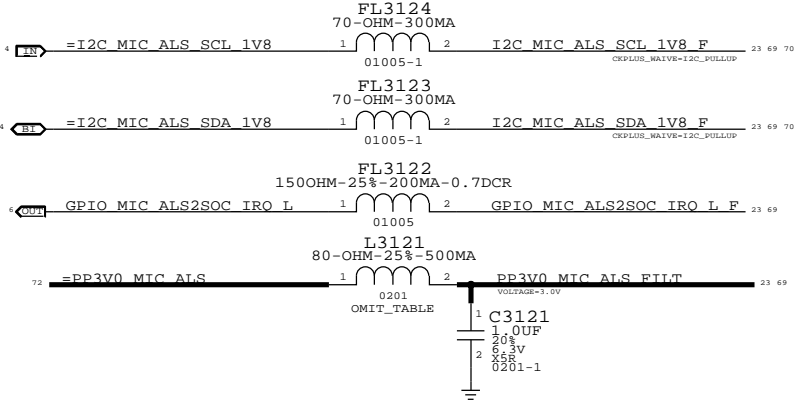
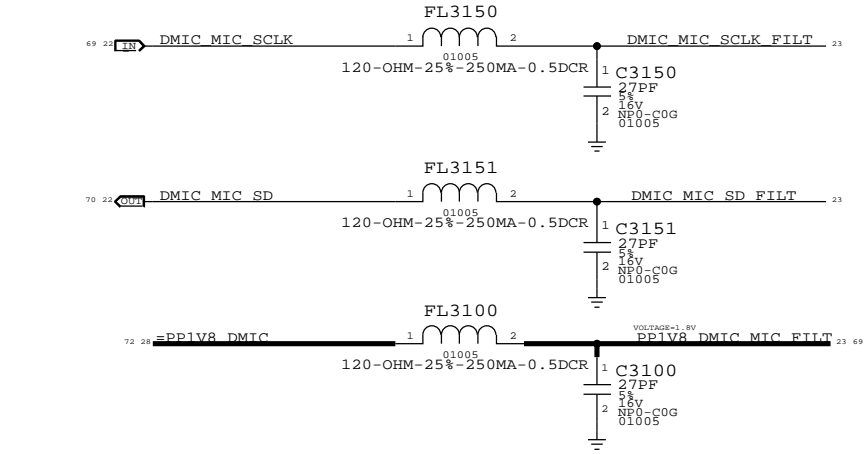
SHUNT FILTERS



MIC FLEX CONNECTOR

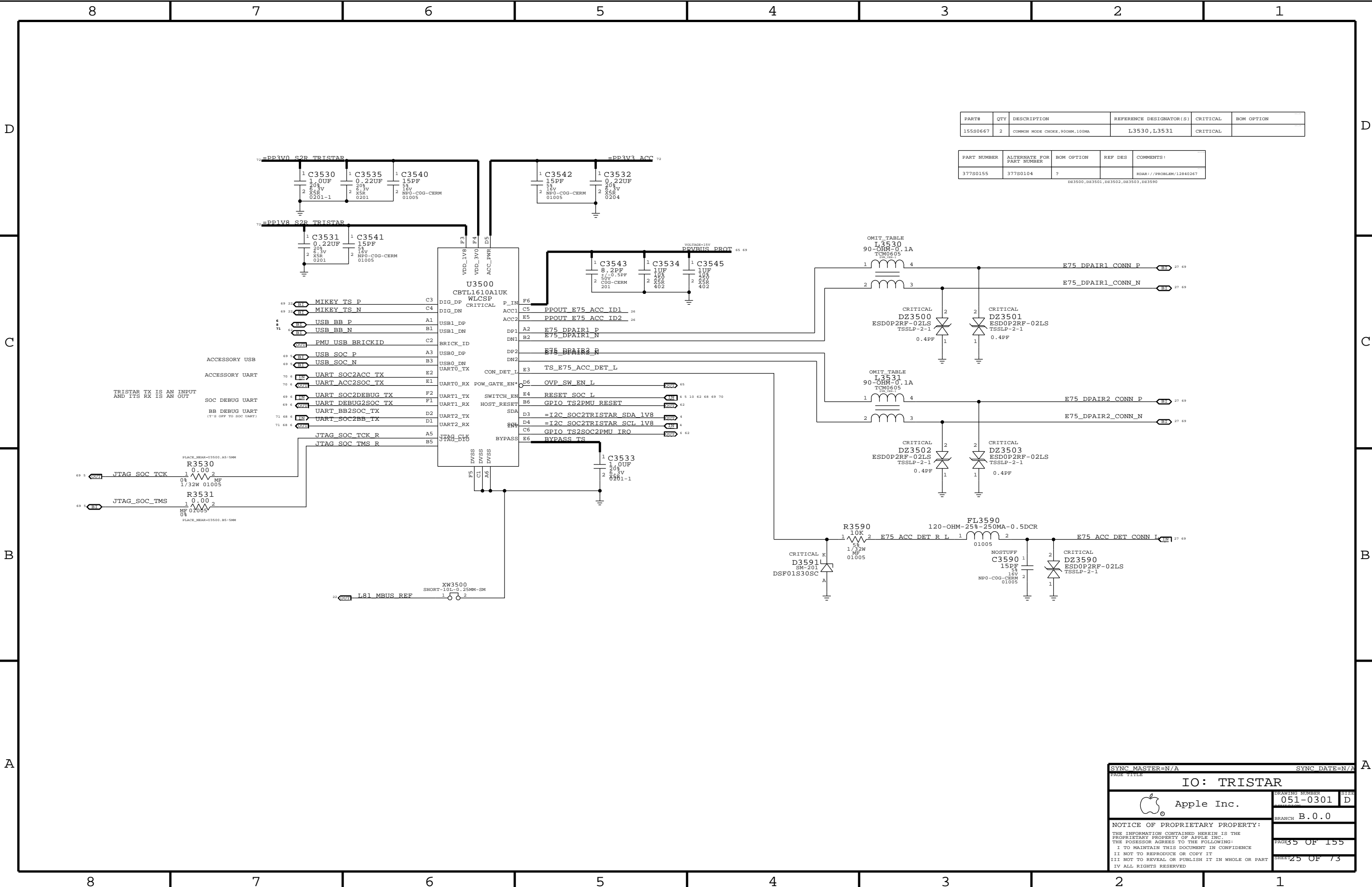


DMIC FILTERS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00018	1	FERRITE, 80OHM, 25%, 500MA, 0.18DCR	L3121	CRITICAL	


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AUDIO: HP/DMIC FLEX CONNS			
Apple Inc.		DRAWING NUMBER	051-0301
		SIZE	D
		BRANCH	B.0.0
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PAGE		31 OF 155	
SHEET		23 OF 73	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0667	2	COMMON MODE CHOKE,90OHM,10DMA	L3530,L3531	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0155	377S0104	?		RDAR: // PROBLEM/12840267

DZ3500,DZ3501,DZ3502,DZ3503,DZ3590

SYNC MASTER=N/A		SYNC DATE=N/A	
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 Apple Inc.		DRAWING NUMBER	
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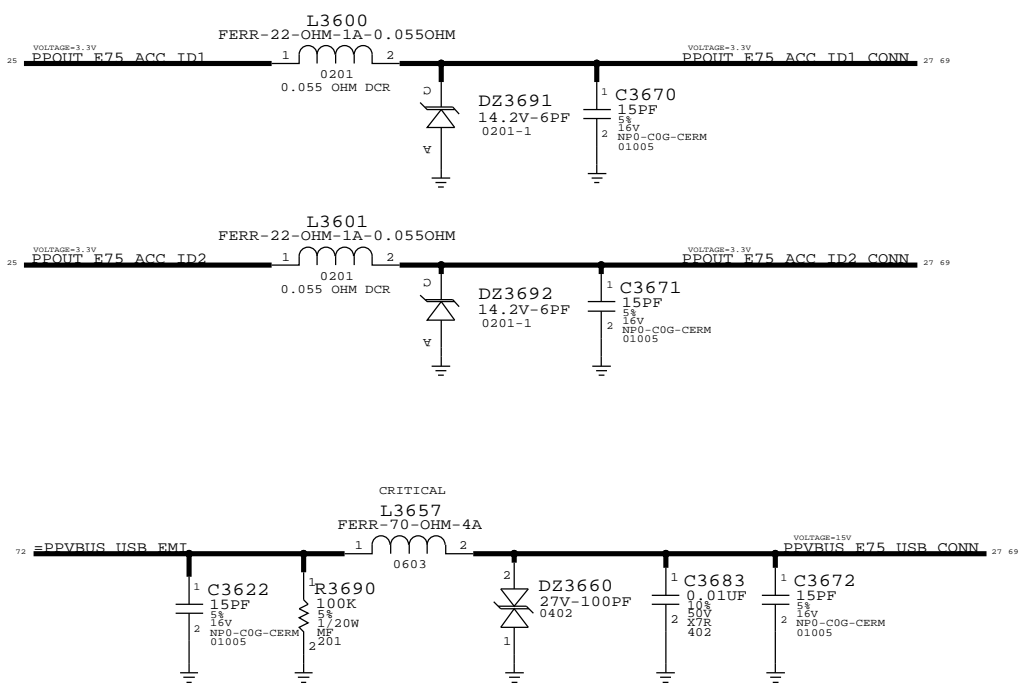
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D

C

B

A




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155S0320	155S0513		L3600, L3601	RDAR:///PROBLEM/9625601
155S0741	155S0397		L3657	RDAR:///PROBLEM/11238851

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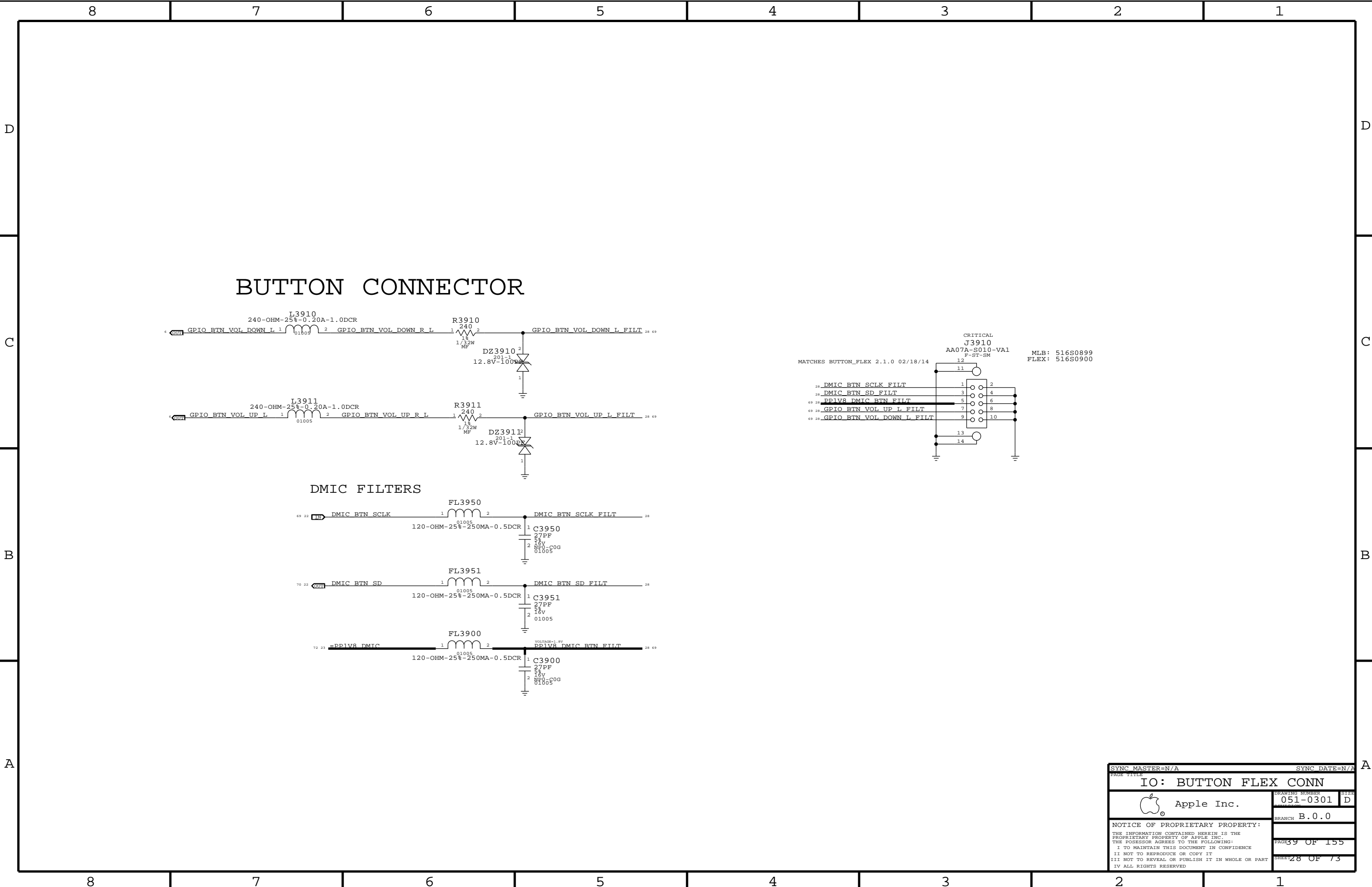
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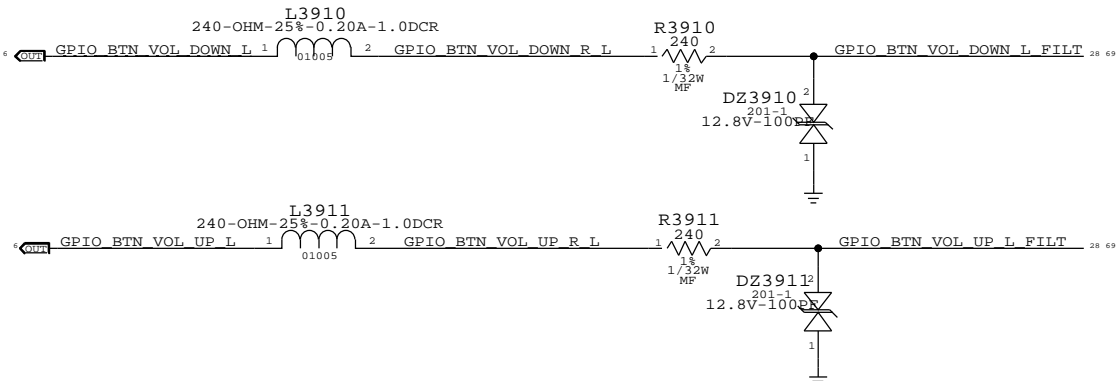
36 OF 155

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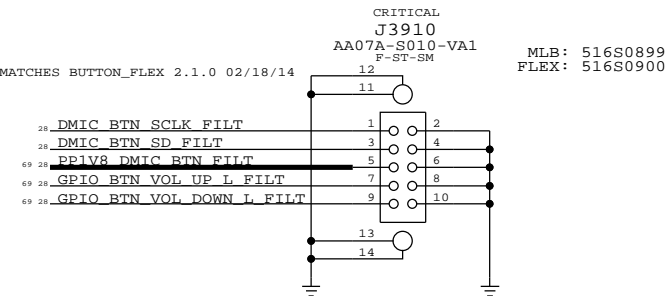
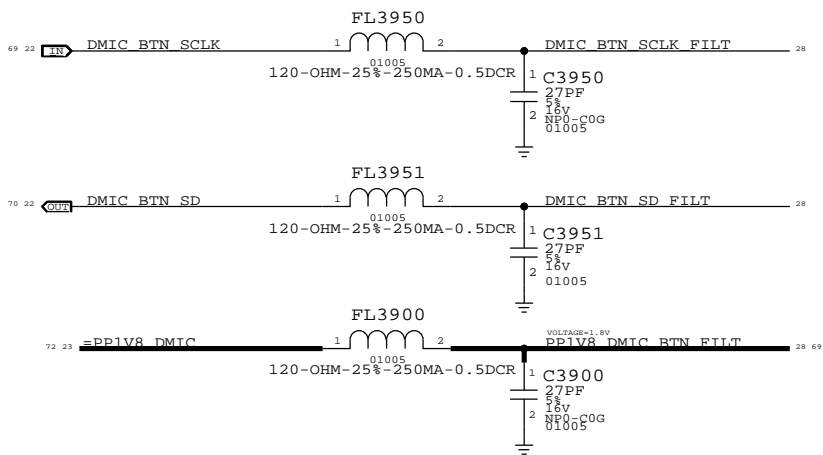
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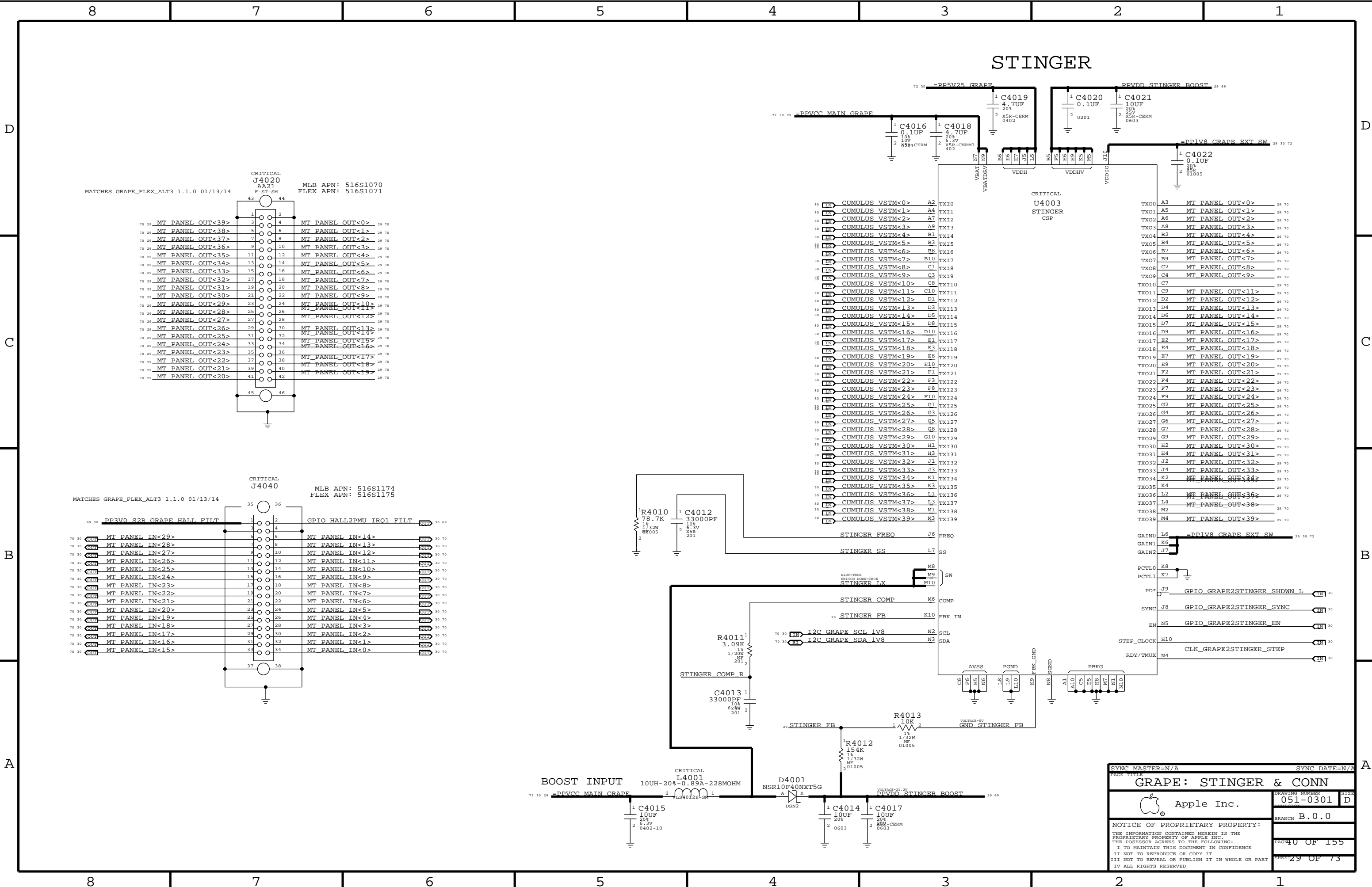



BUTTON CONNECTOR

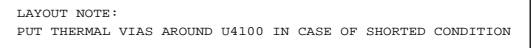


DMIC FILTERS





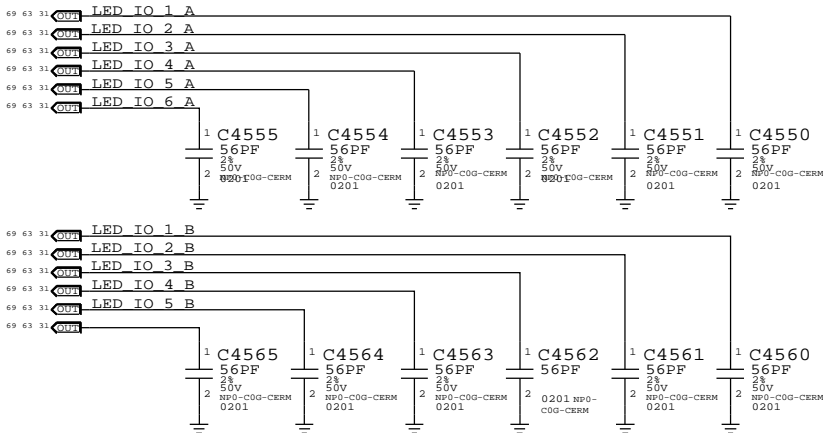
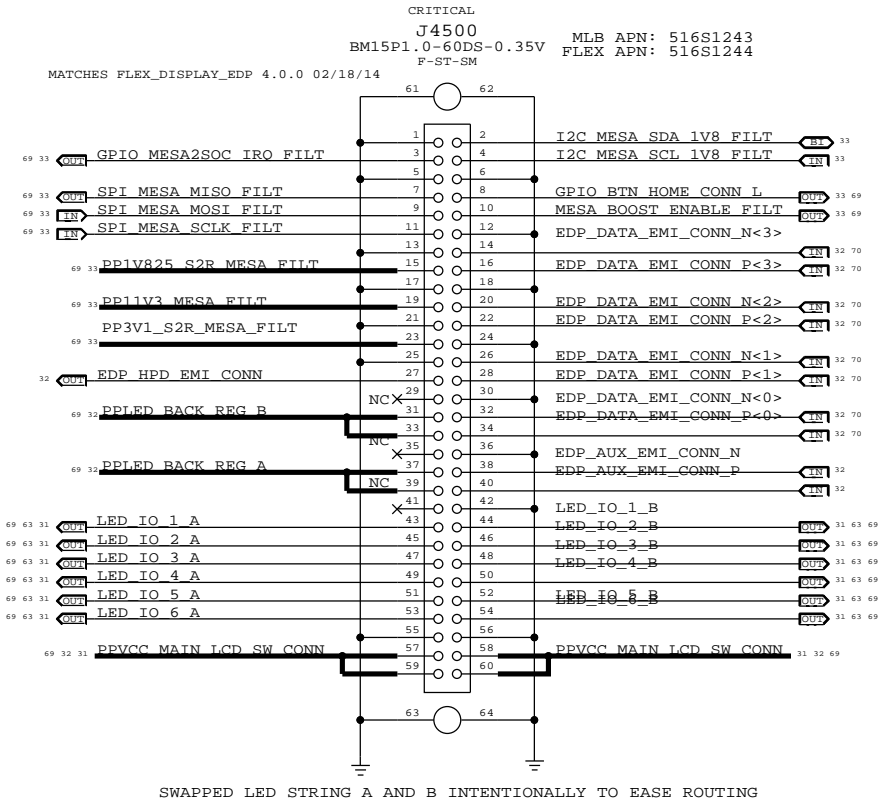
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AA

DISPLAY CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00011	131S0641	?	C4550, ECT	RDAR://PROBLEM/15682101

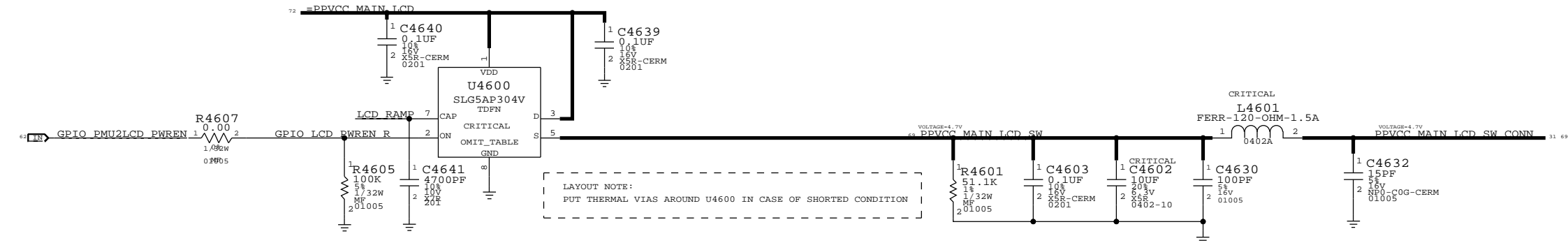
DISPLAY CONNECTOR



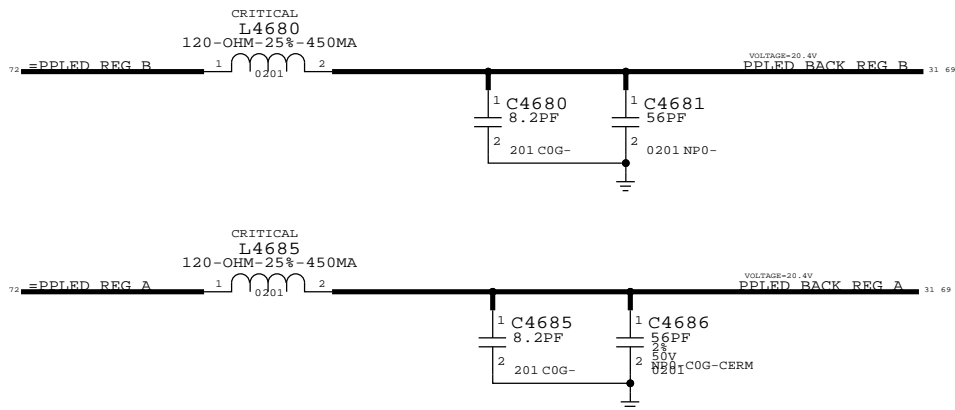
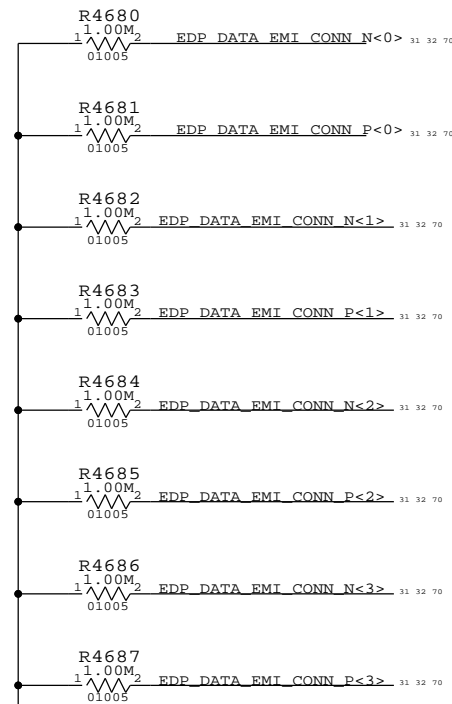
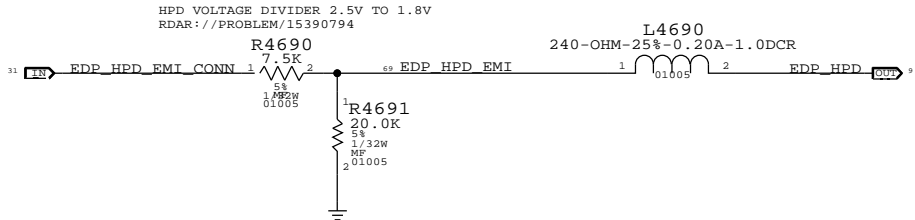
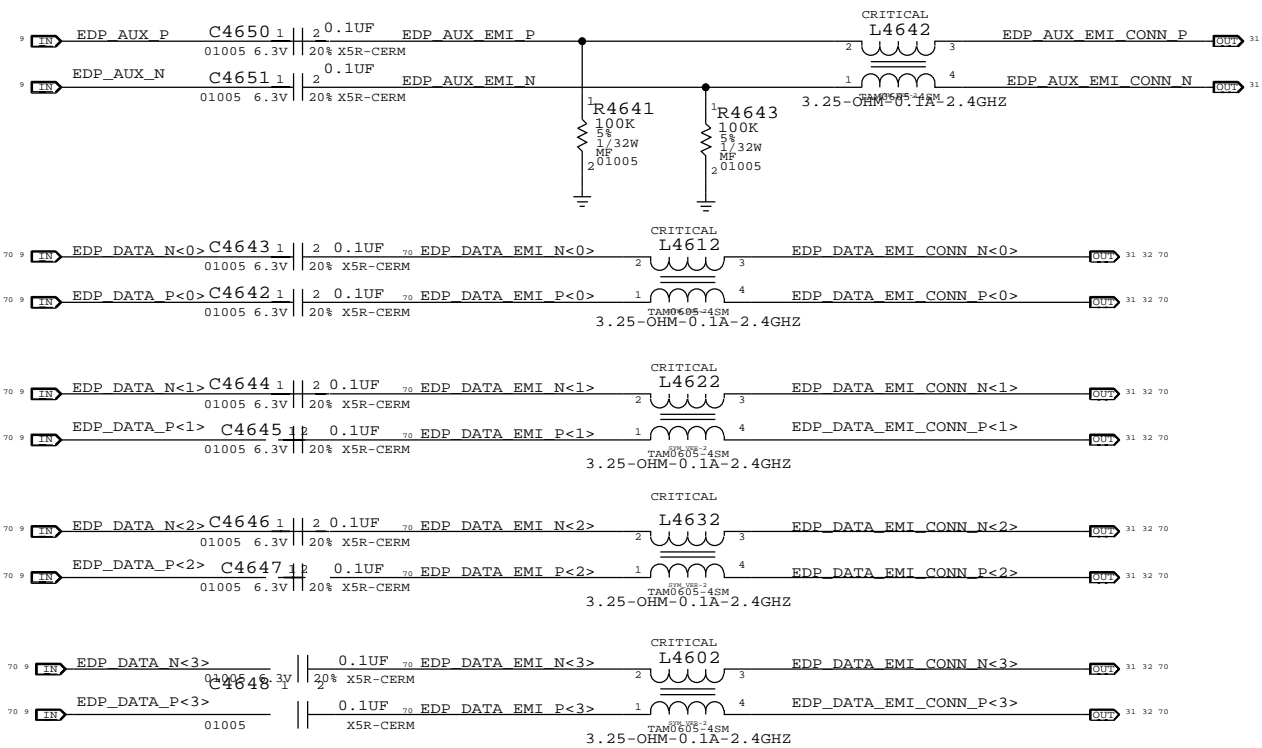
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		PAGE 45 OF 155	
		SHEET 31 OF 73	

EDP CONNECTOR SUPPORT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897	?	L4602, ECT	RDAR:///PROBLEM/15954071



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4600	CRITICAL	?

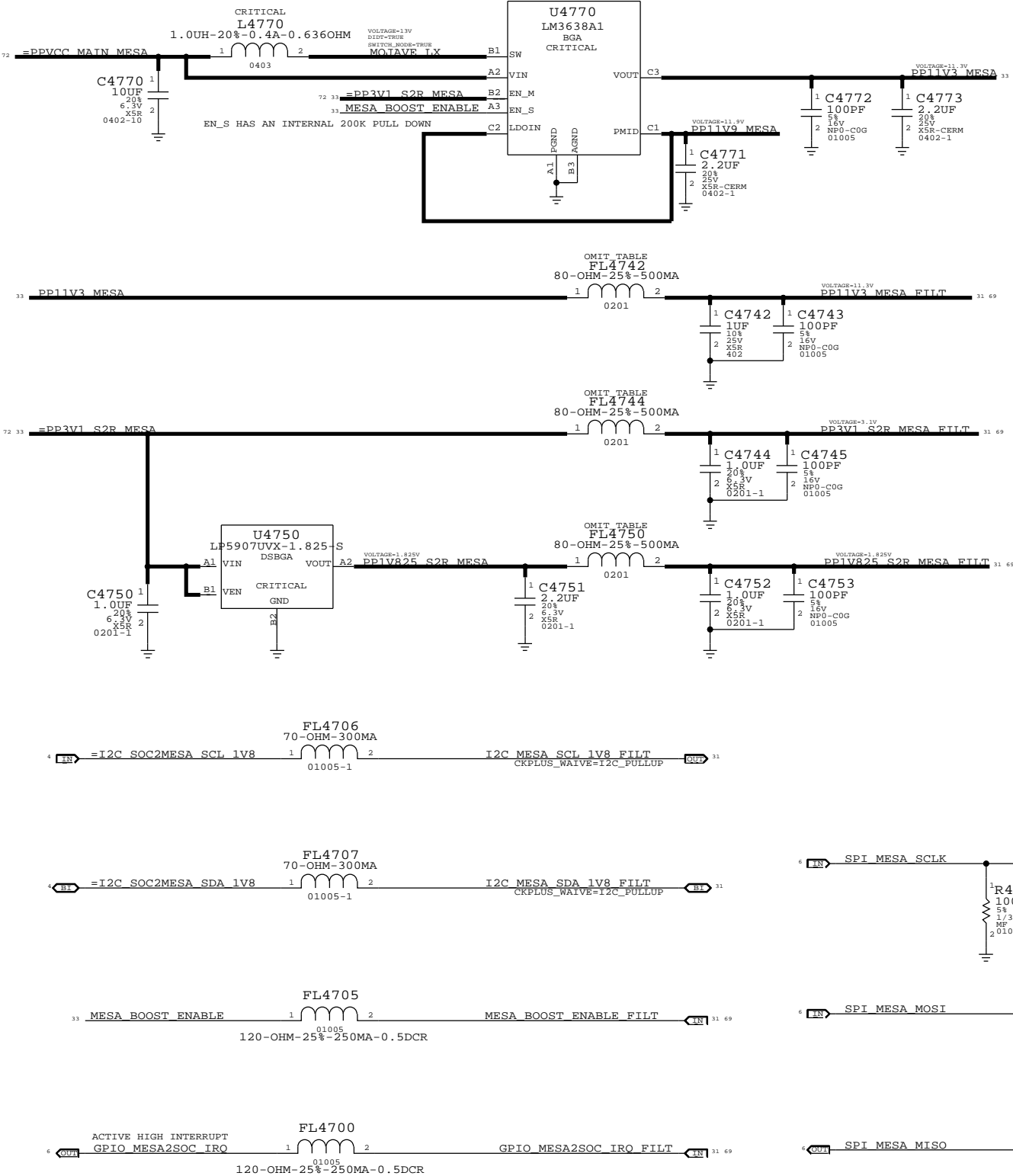


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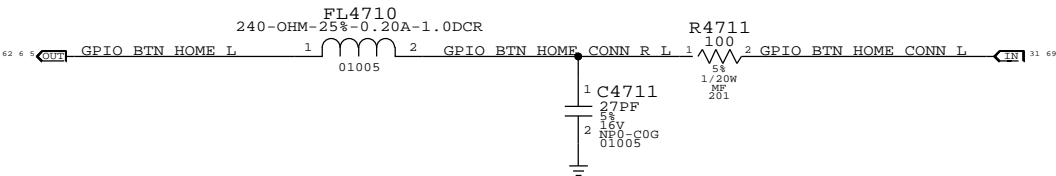
MESA & HOME BUTTON

MOJAVE

USING A1 BECAUSE NAVAJO NEEDS 11V3



HOME BUTTON FILTERS




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155S00017	155S0755			RDAR://PROBLEM/15807137

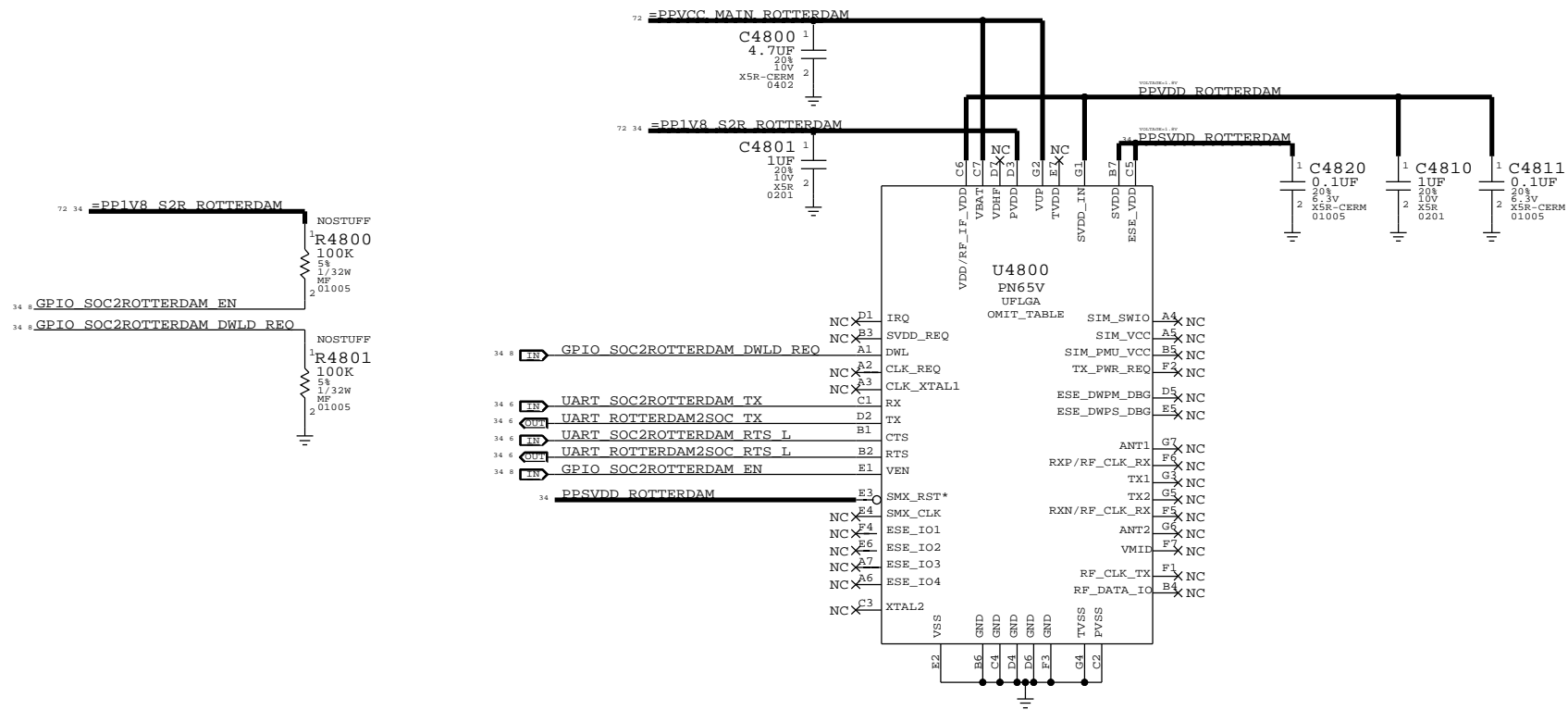
FL3910, FL3911, FL4124, L4690, FL4710

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00018	155S0664			RDAR://PROBLEM/15796569

FL2800, FL2802, FL2803, FL2861, FL2871, FL2881, FL2891, FL4742, FL4744, FL4750, FL7900

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MESA: SUPPORT			
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		BRANCH	B.0.0
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J82 - ROTTERDAM



PP4800	0.5M	1	UART_SOC2ROTTERDAM_TX	6	34
PP4801	1.5M	1	UART_ROTTERDAM2SOC_TX	6	34
PP4802	2.5M	1	UART_SOC2ROTTERDAM_RTS_L	6	34
PP4803	3.5M	1	UART_ROTTERDAM2SOC_RTS_L	6	34
PP4804	4.5M	1	GPIO_SOC2ROTTERDAM_EN	8	34
PP4806	6.5M	1	GPIO_SOC2ROTTERDAM_DWLD_REQ	8	34

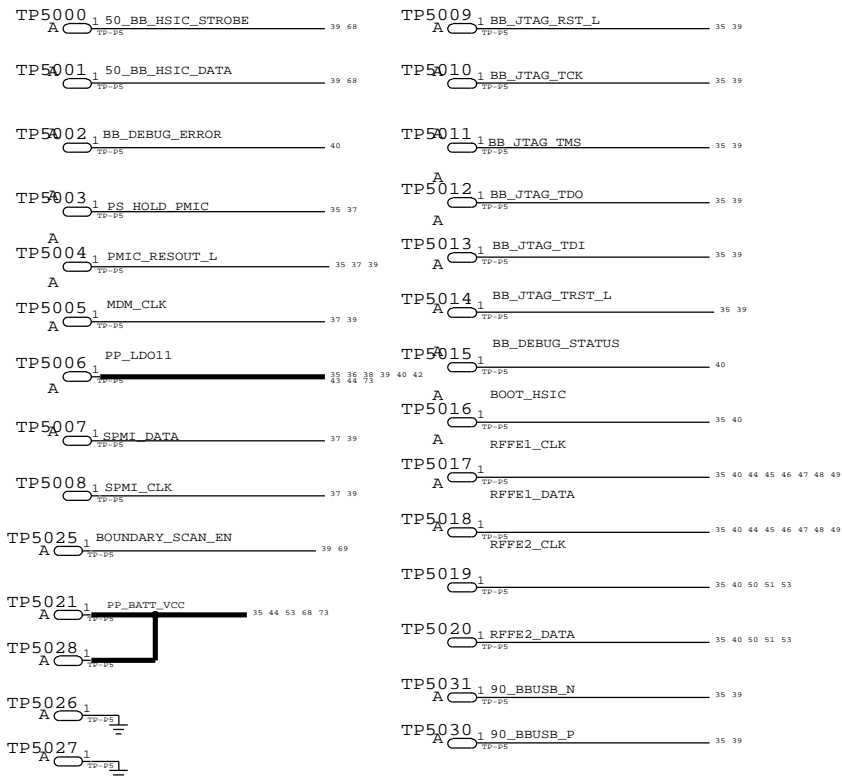
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338S00043	1	IC,ROTTERDAM,MP,UFLGA49	U4800	CRITICAL	

PAGE TITLE		
ROTTERDAM		
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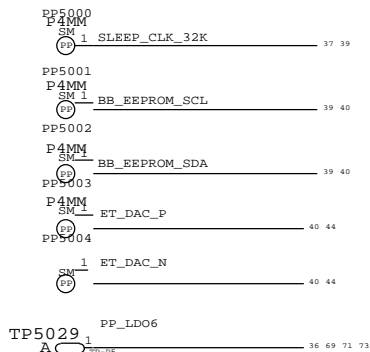
AP INTERFACE & DEBUG CONNECTOR

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TEST POINTS



PROBE POINTS

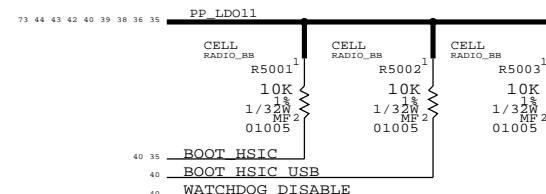
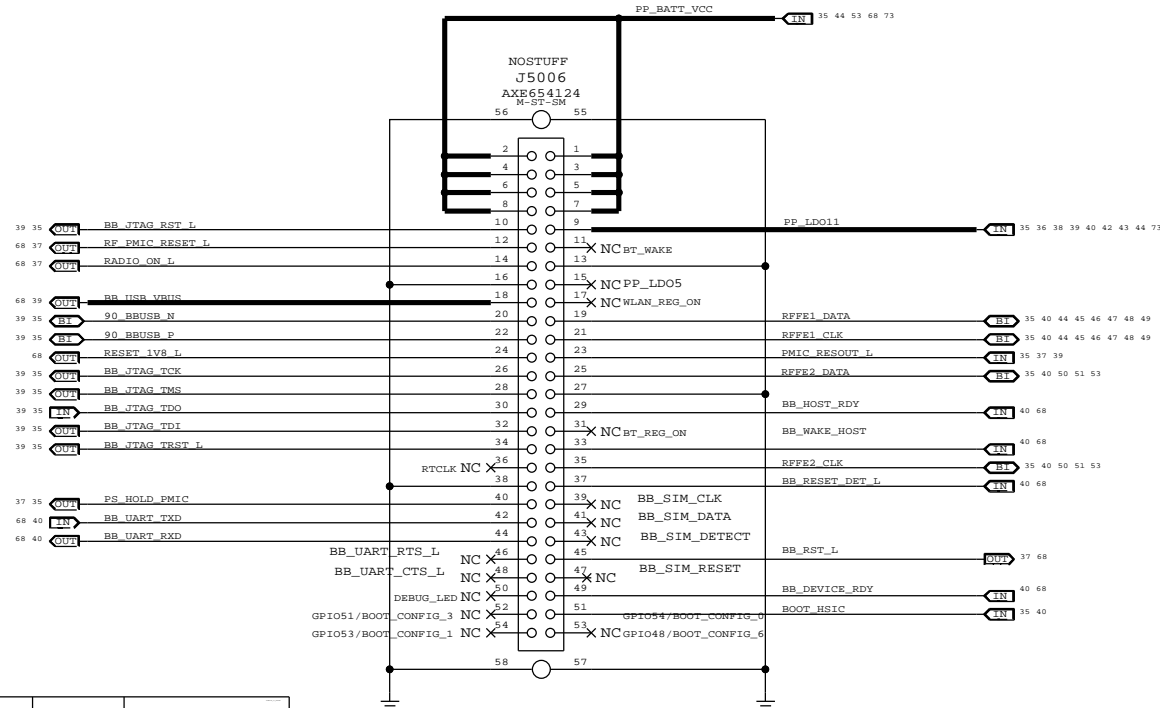


CONFIG_RF BOM OPTIONS

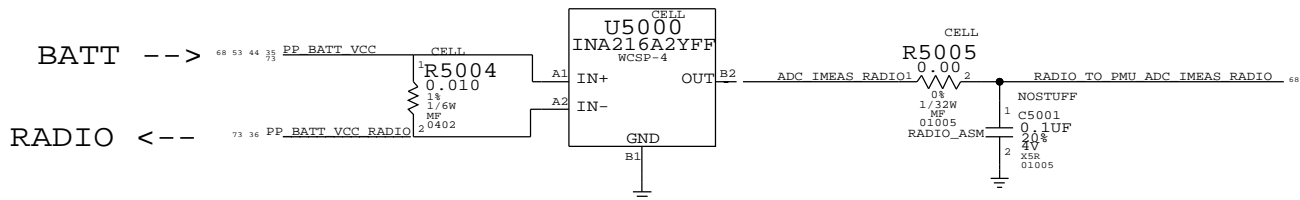
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131S0273	1	0.8PF 0201	C6001	CRITICAL	X202_RF
131S0431	1	0.2PF 0201	C6013	CRITICAL	X190_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X202_RF
152S2020	1	3.6NH +/-0.1NH 400MA 0201	L6001	CRITICAL	X190_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X137_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X202_RF
131S0323	1	1.1PF 0201	C6421	CRITICAL	X190_RF
152S1217	1	1.0NH +/-0.1NH 750MA 0201	L6402	CRITICAL	X190_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X137_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X202_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X190_RF
152S1977	1	10.0NH 3% 170MA 01005	C6202	CRITICAL	X137_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X202_RF
152S00028	1	22NH 3% 120MA 01005	L6720	CRITICAL	X190_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X137_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X202_RF
138S0831	5	MURATA 2.2UF CAPACITOR	CS101,CS121,CS122,C6010,C6011	CRITICAL	CELL

REPLACES 138S0917, 138S0917, CAN ONLY BE USED ON RAILS WITH 3V OR LESS

DEBUG CONNECTOR




PP_VCC_MAIN CURRENT SENSE



BOM ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1850	152S1721		L6001,L6103,L6104	MURATA IN, 2.2UF, 2016
152S2050	152S1857		L5902	TAIYO IND, 2.2UF, 2012

REVISION DATE: 9/29/2014

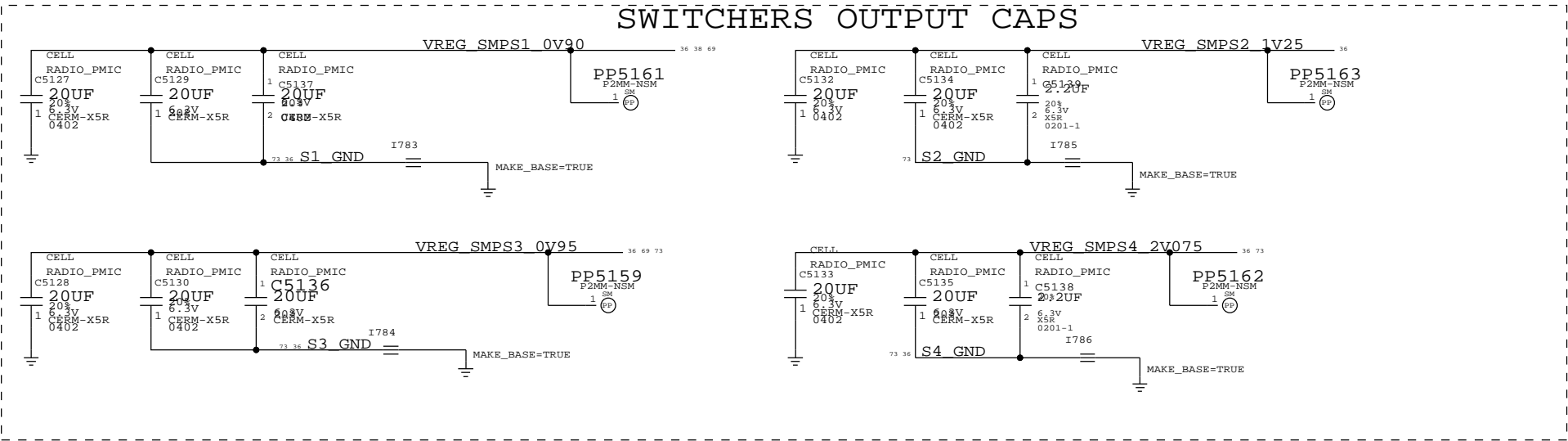
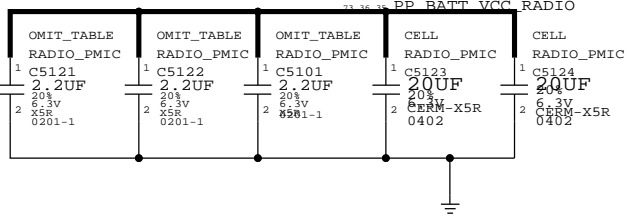
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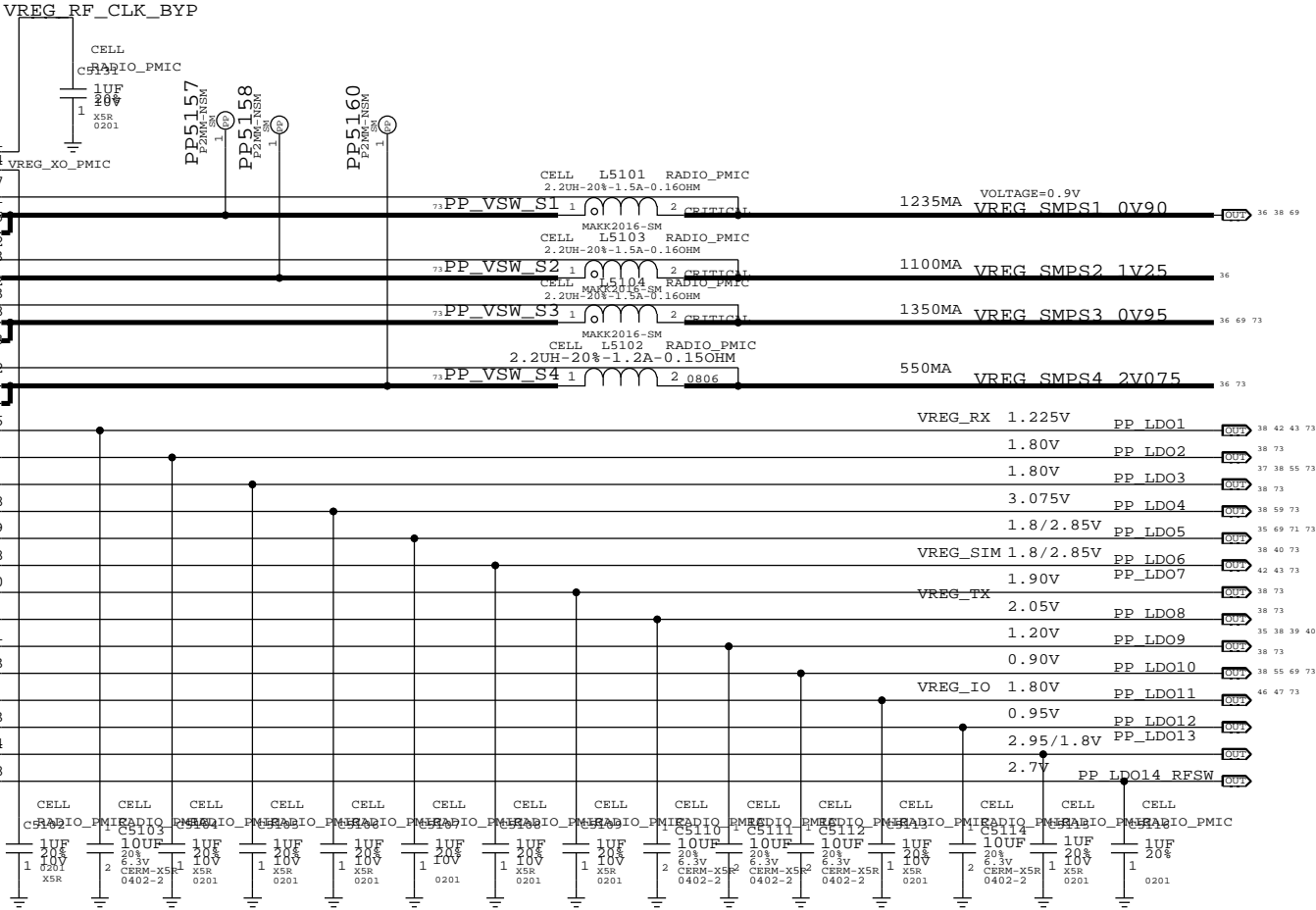
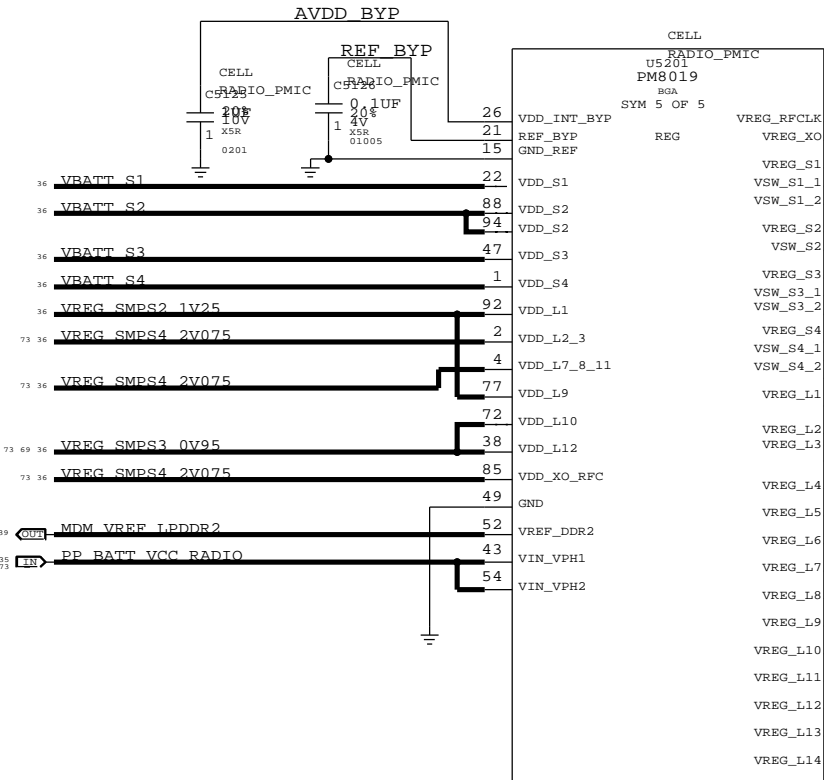
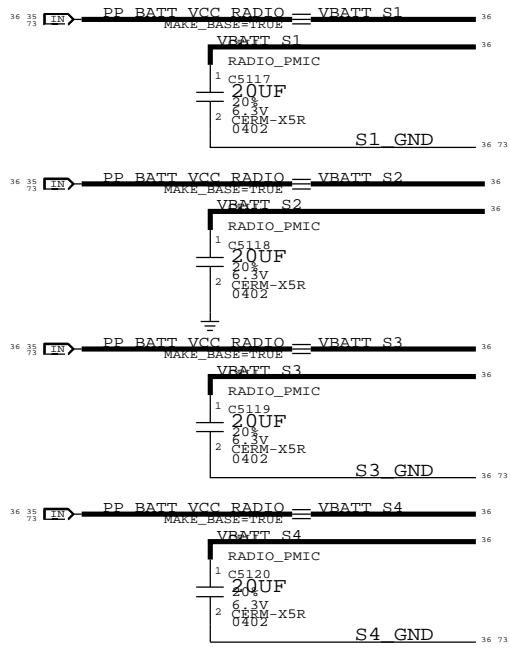
BASEBAND PMU (1 OF 2)

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C332
R302
L304
U301



SWITCHERS BULK CAPS



CELL: BB PMU (1/2)



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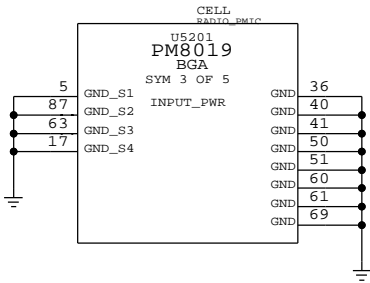
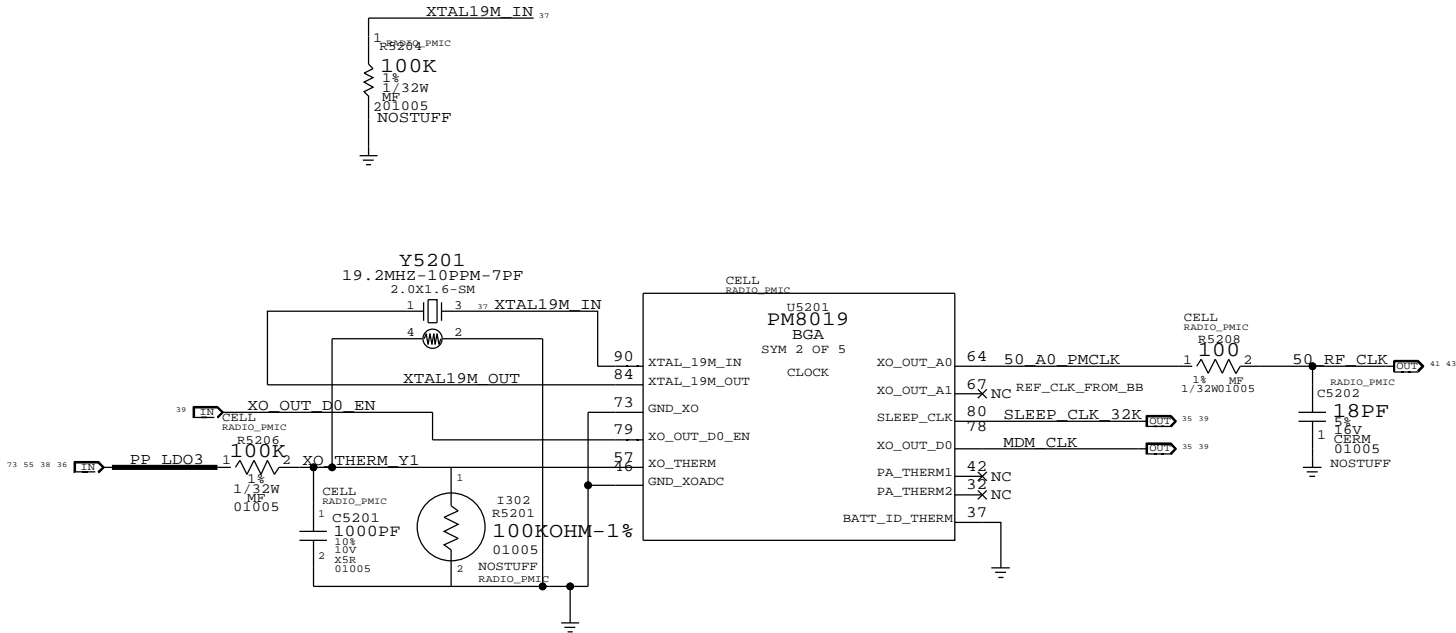
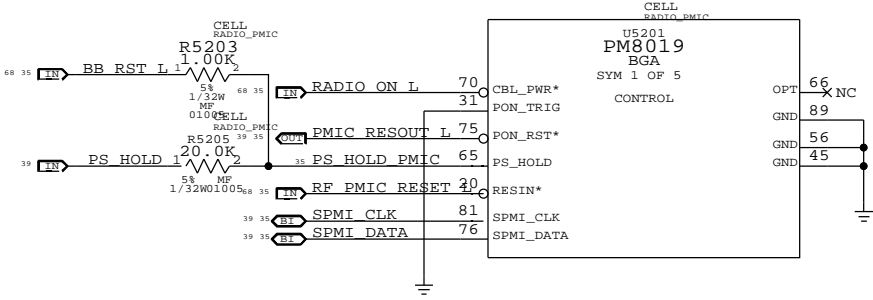
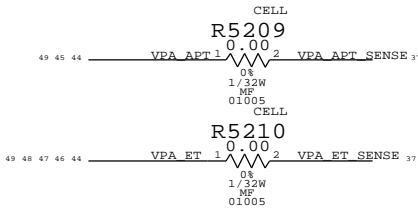
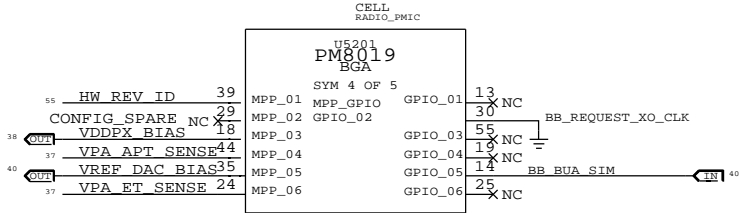
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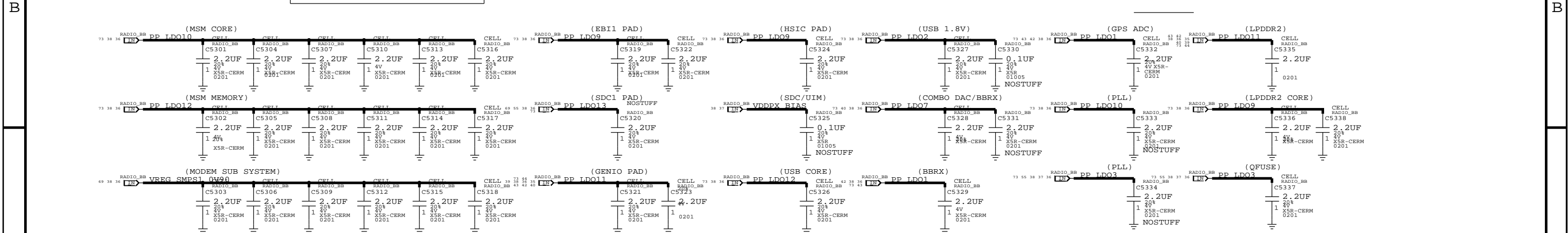
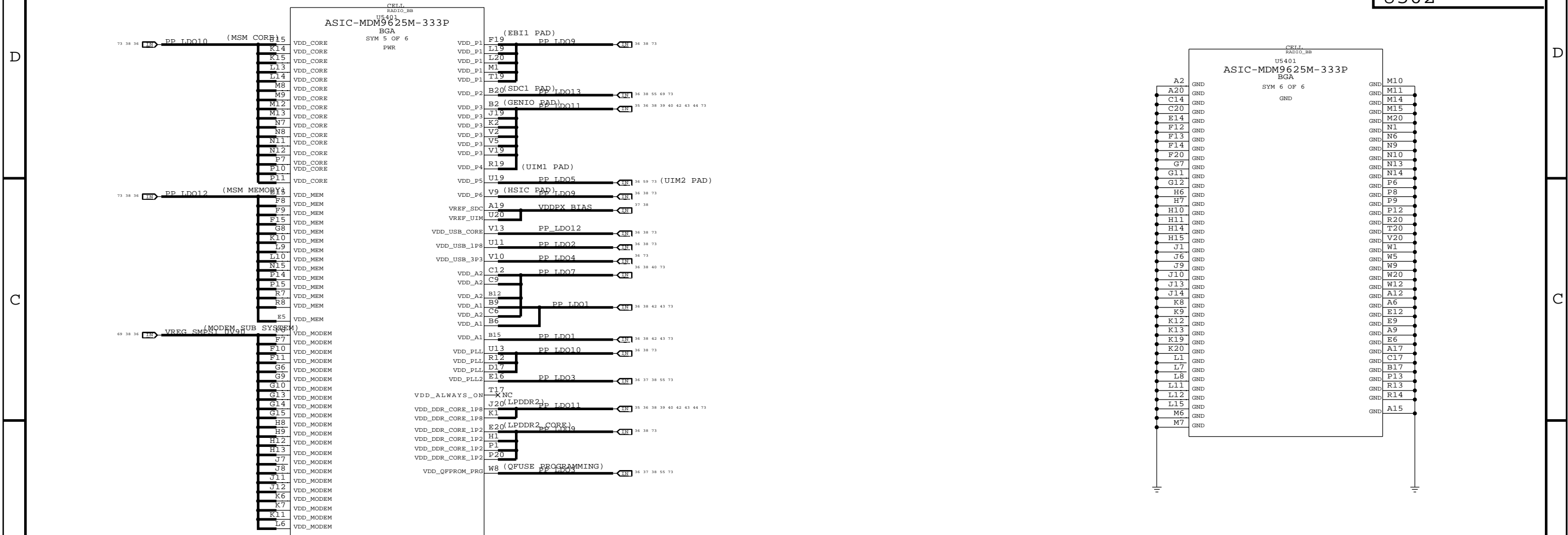
C401
R411
L400
U404

HW_REV_ID	R5202	R5207	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	N/A
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO0
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO1
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	EVT		
0.60V	102K	51.1K	DVT		
0.70V	82.5K	51.1K	PVT		



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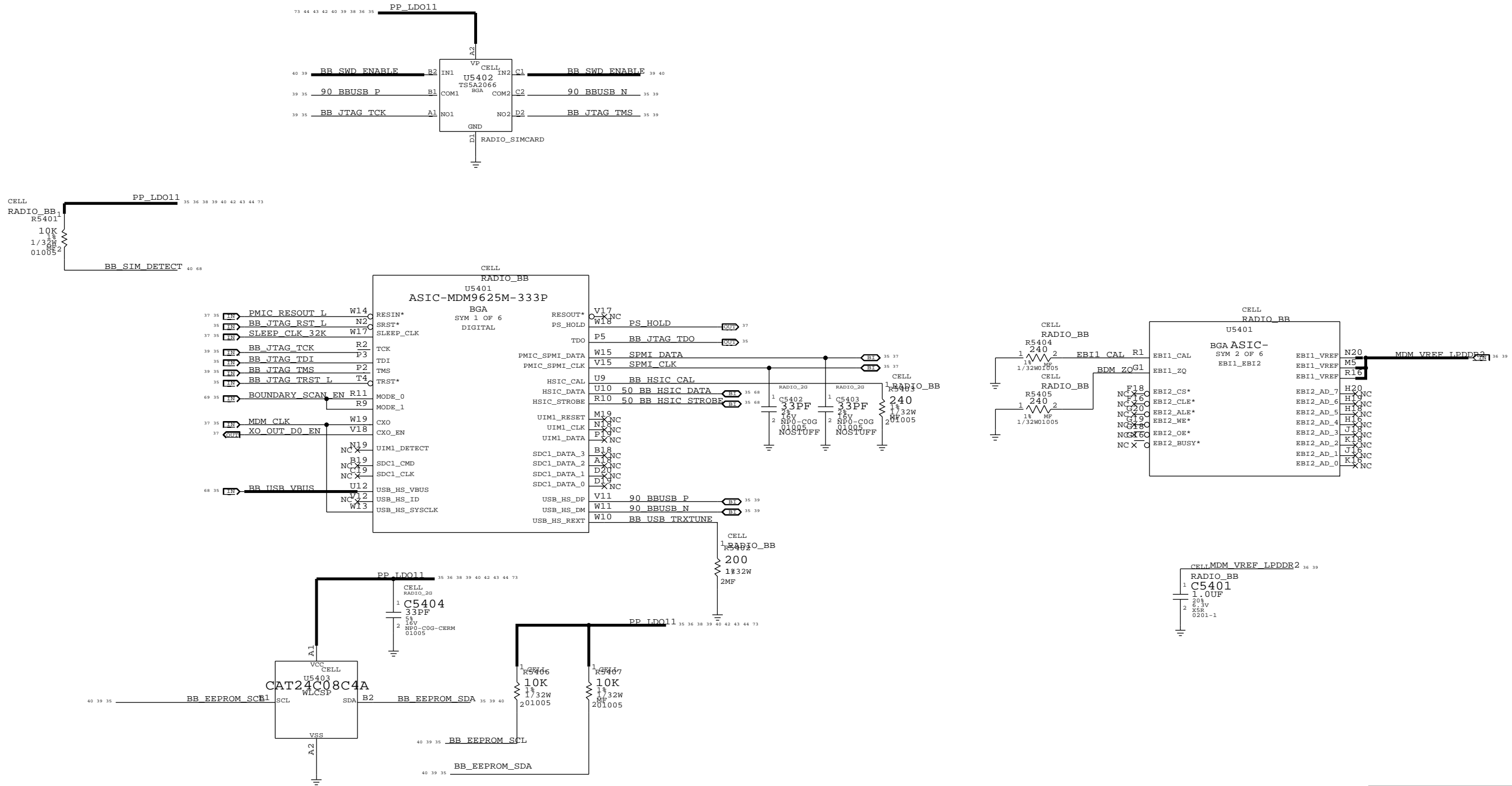
C538
R500
L500
U502



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C600
R606
L600
U602

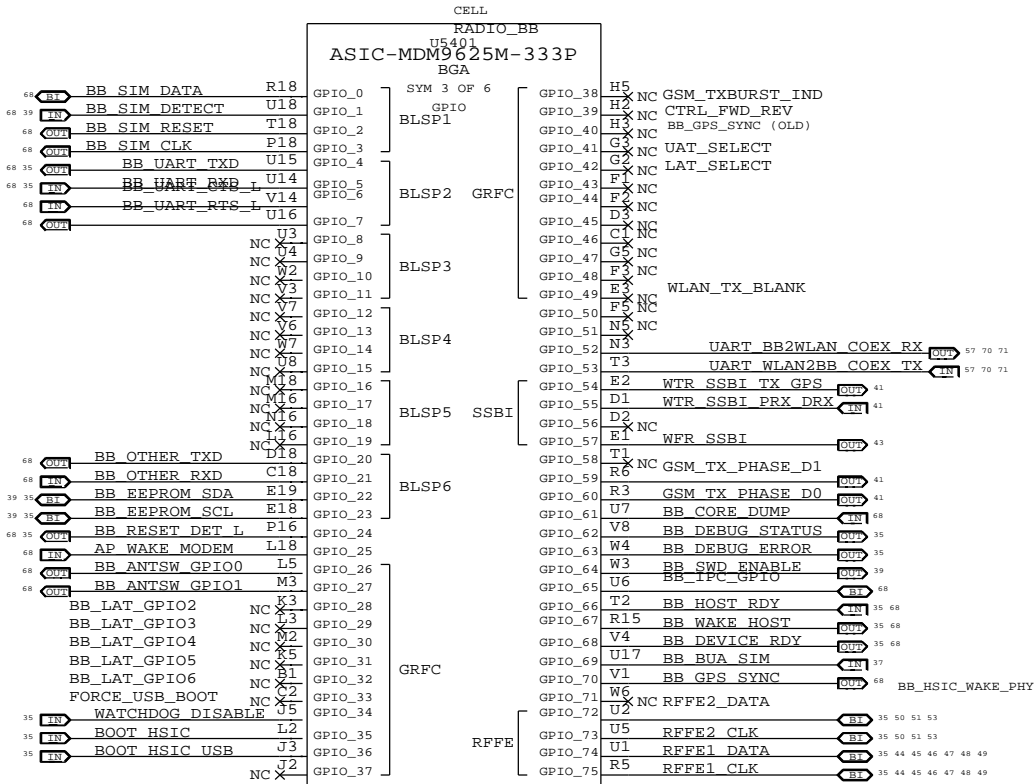
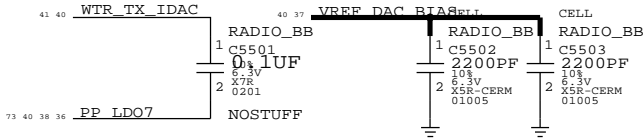
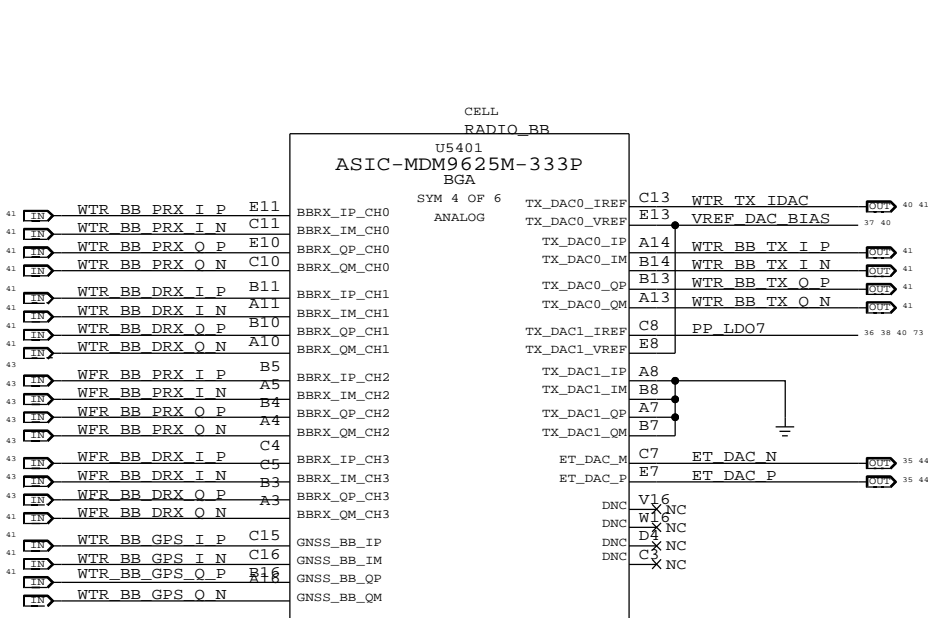


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C704

U702



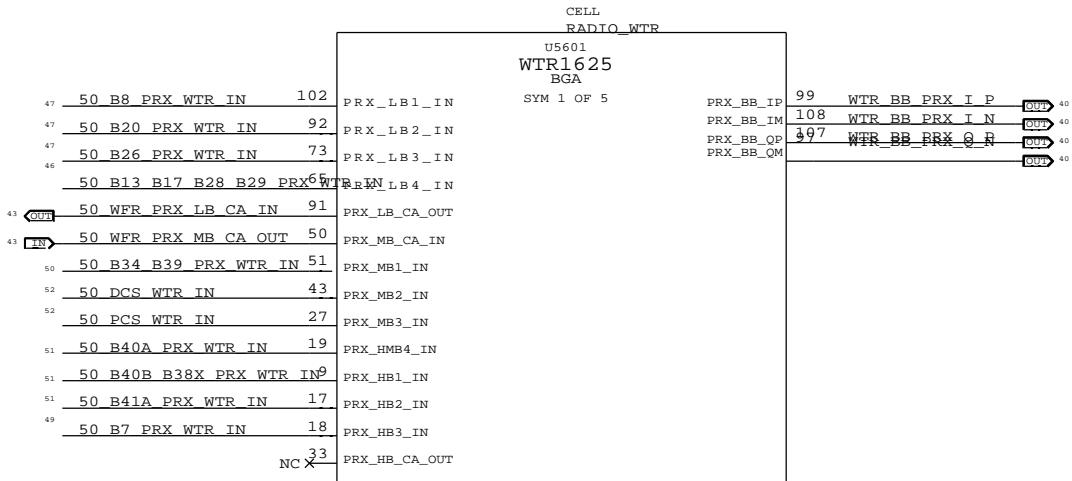
I447
PP_LDO11 RFFE_VIO

WTR TRANSCEIVER (1 OF 2)

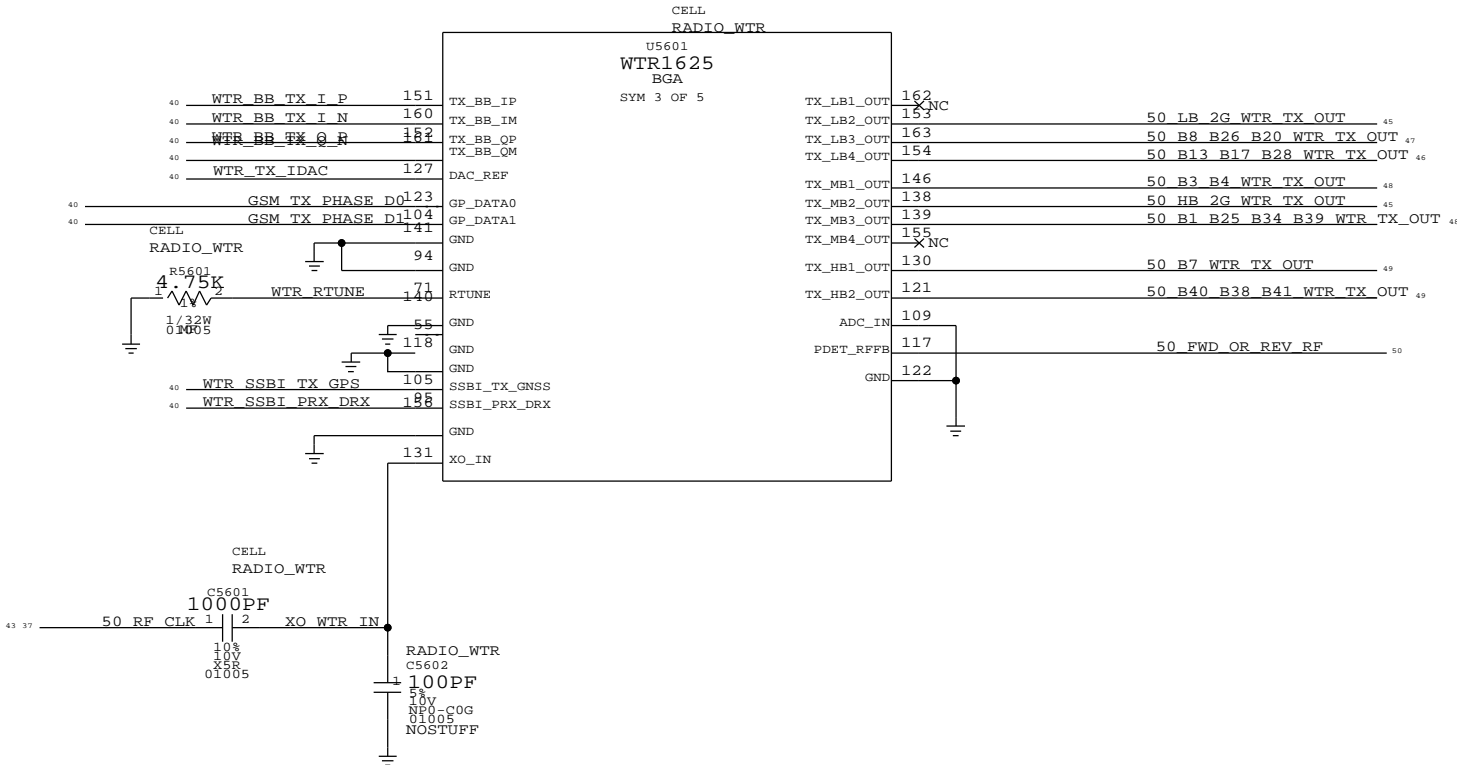
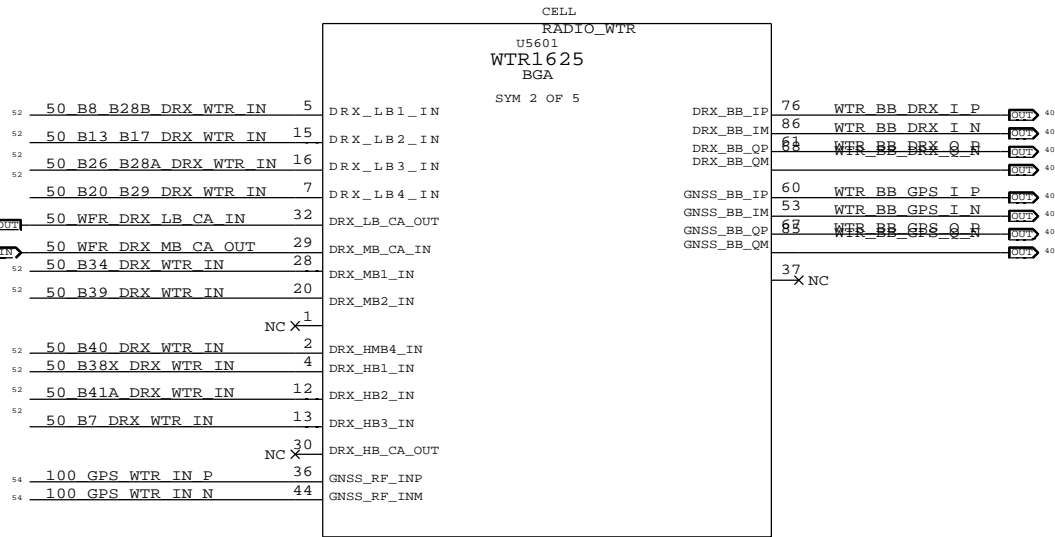
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C802
R802
L800
U803

LB1	DC
LB2	DC
LB3	DC
LB4	DC
MB1	NO DC
MB2	DC
MB3	DC
HB1	NO DC
HB2	DC
HB3	DC
HMB4	NO DC



LB1	DC
LB2	DC
LB3	DC
LB4	DC
MB1	NO DC
MB2	DC
MB3	DC
HB1	NO DC
HB2	DC
HB3	DC
HMB4	NO DC



RF_CLK IS SHARED BETWEEN WTR AND WFR. LENGTH DIFFERENCE BETWEEN THE TWO SHOULD BE < 5MM.

PAGE 1/1111B

CELL: RF TXCVR (1/3)

Apple Inc.

051-0301 D

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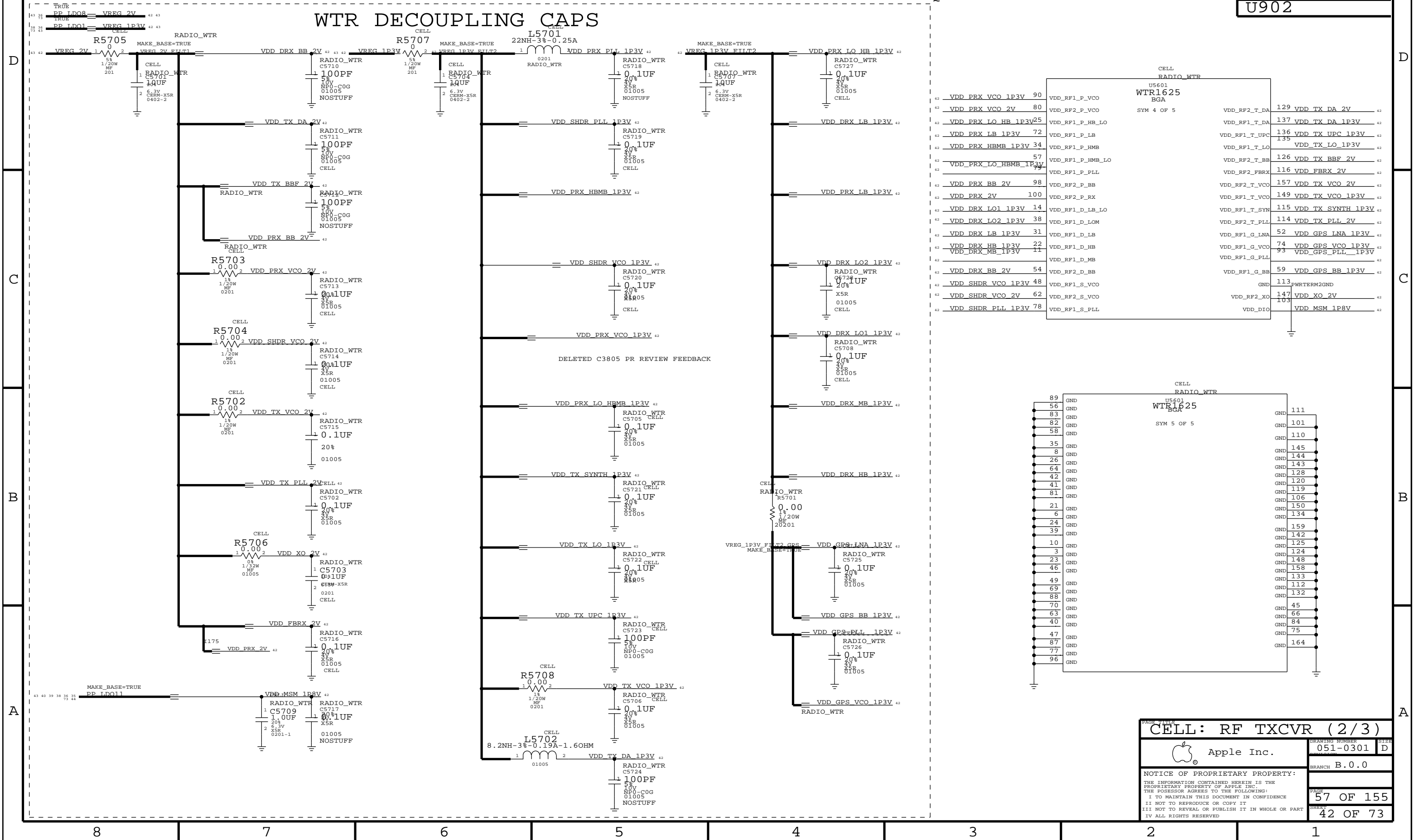
56 OF 155
41 OF 73

WTR TRANSCEIVER (2 OF 2)

~~CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.~~

C934
R926
L3802_RF
U902

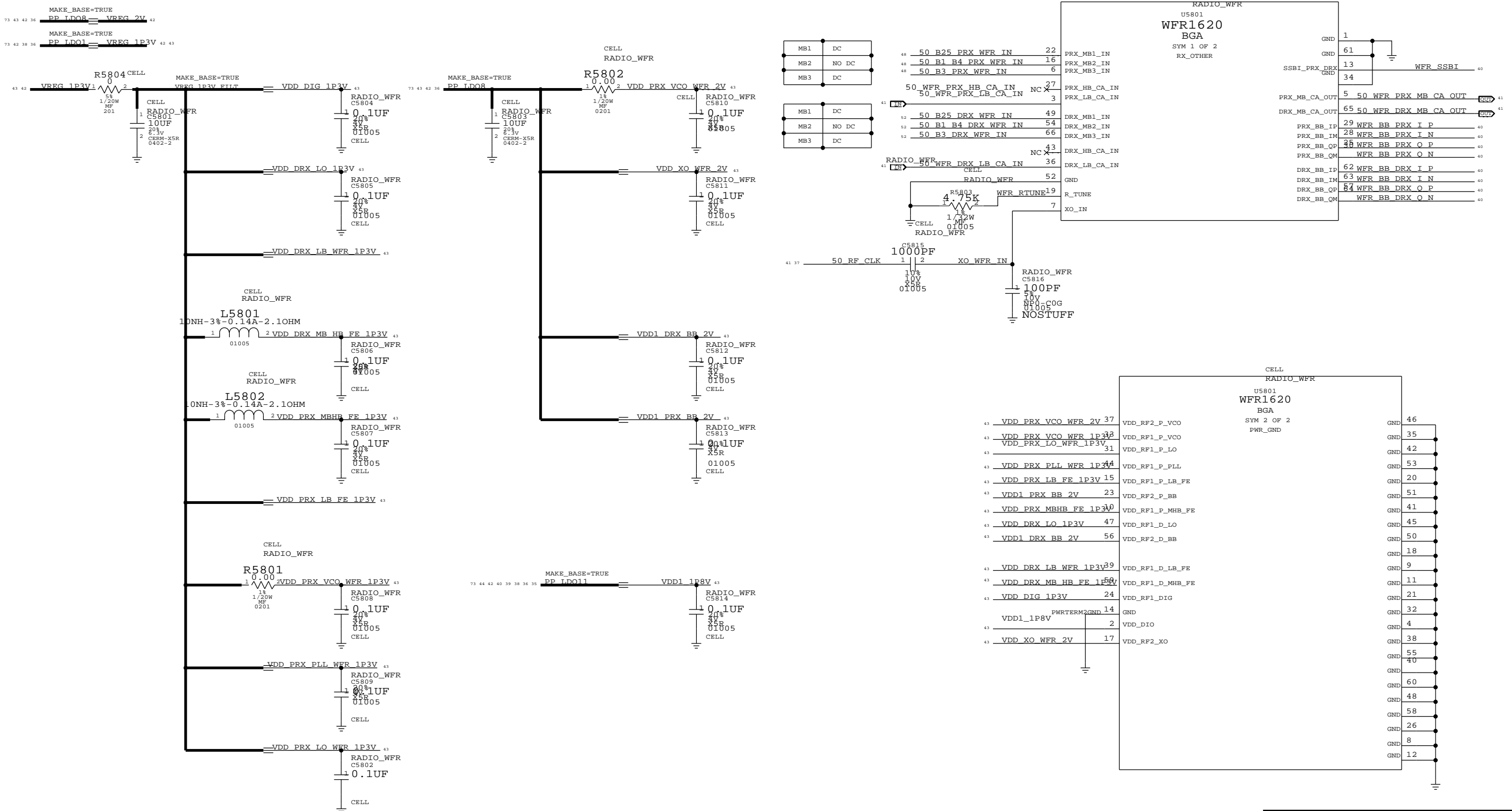
WTR DECOUPLING CAPS



WFR TRANSCEIVER

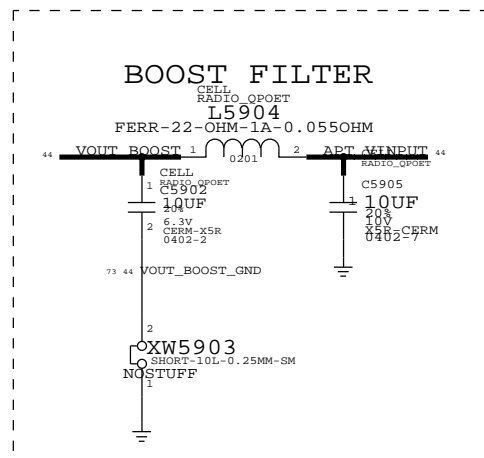
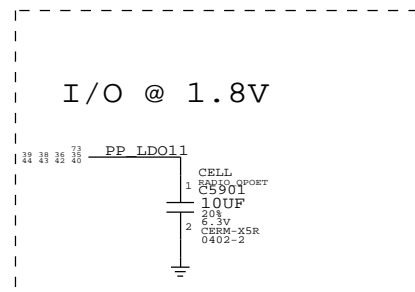
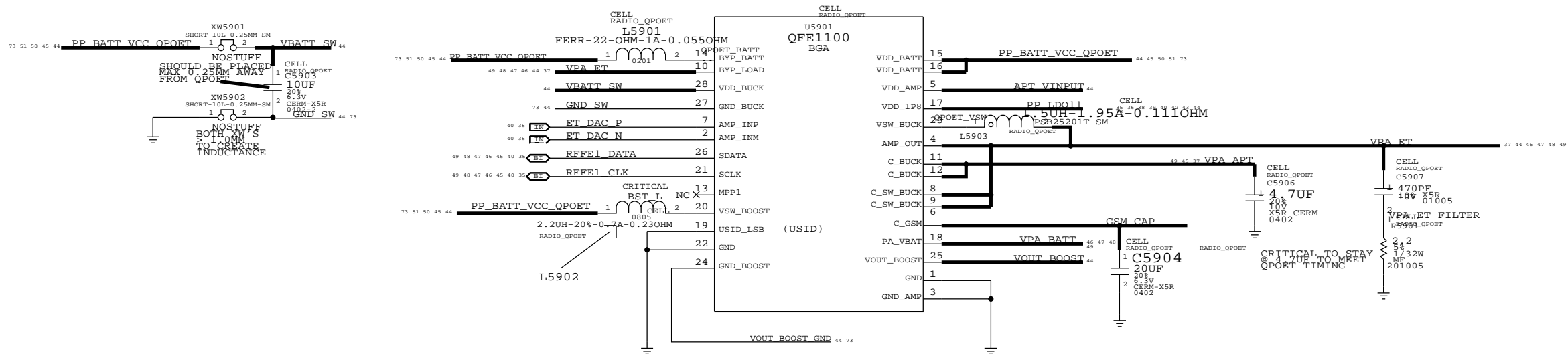
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

C1019
R1016
L1000
U1002

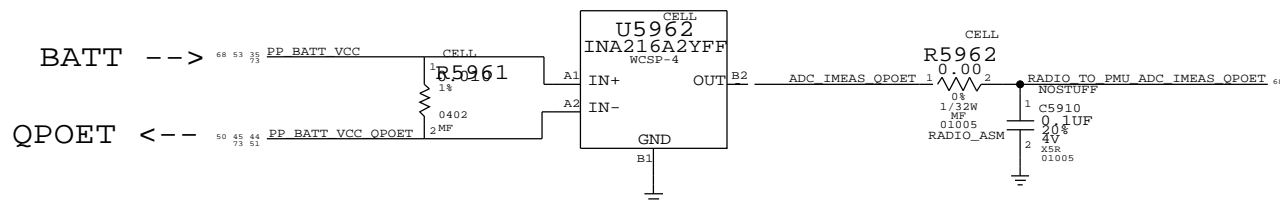



~~CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.~~

C11110
R1102
L1104
U1101



PP_VCC_MAIN CURRENT SENSE



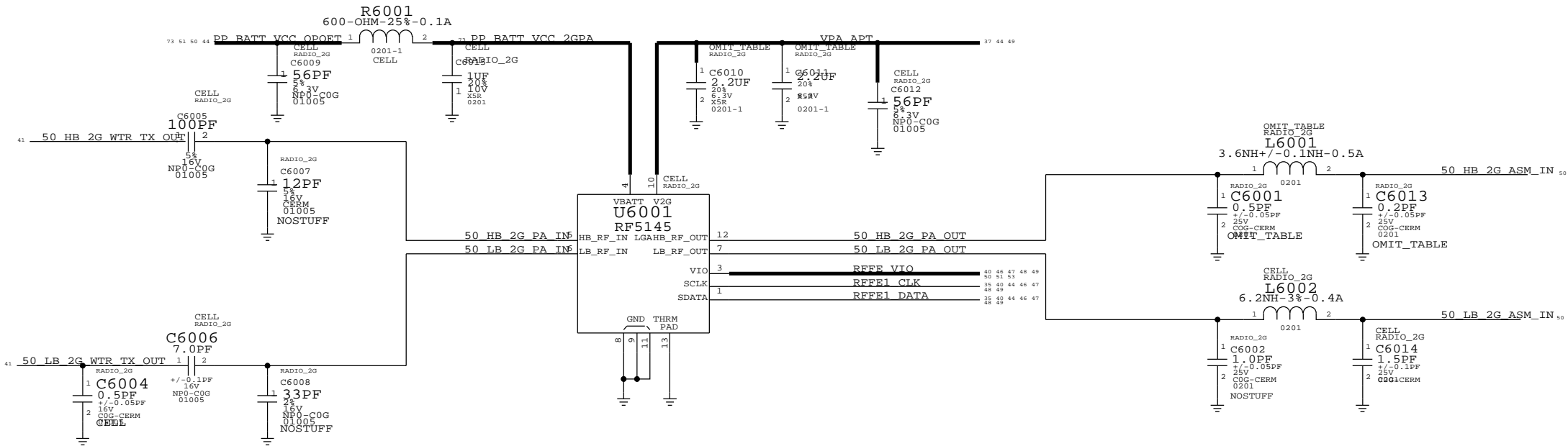
PAGE TITLE		CELL: QFE DCDC	
	Apple Inc.		DRAWING NUMBER 051-0301
			SIZE D
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2G PA

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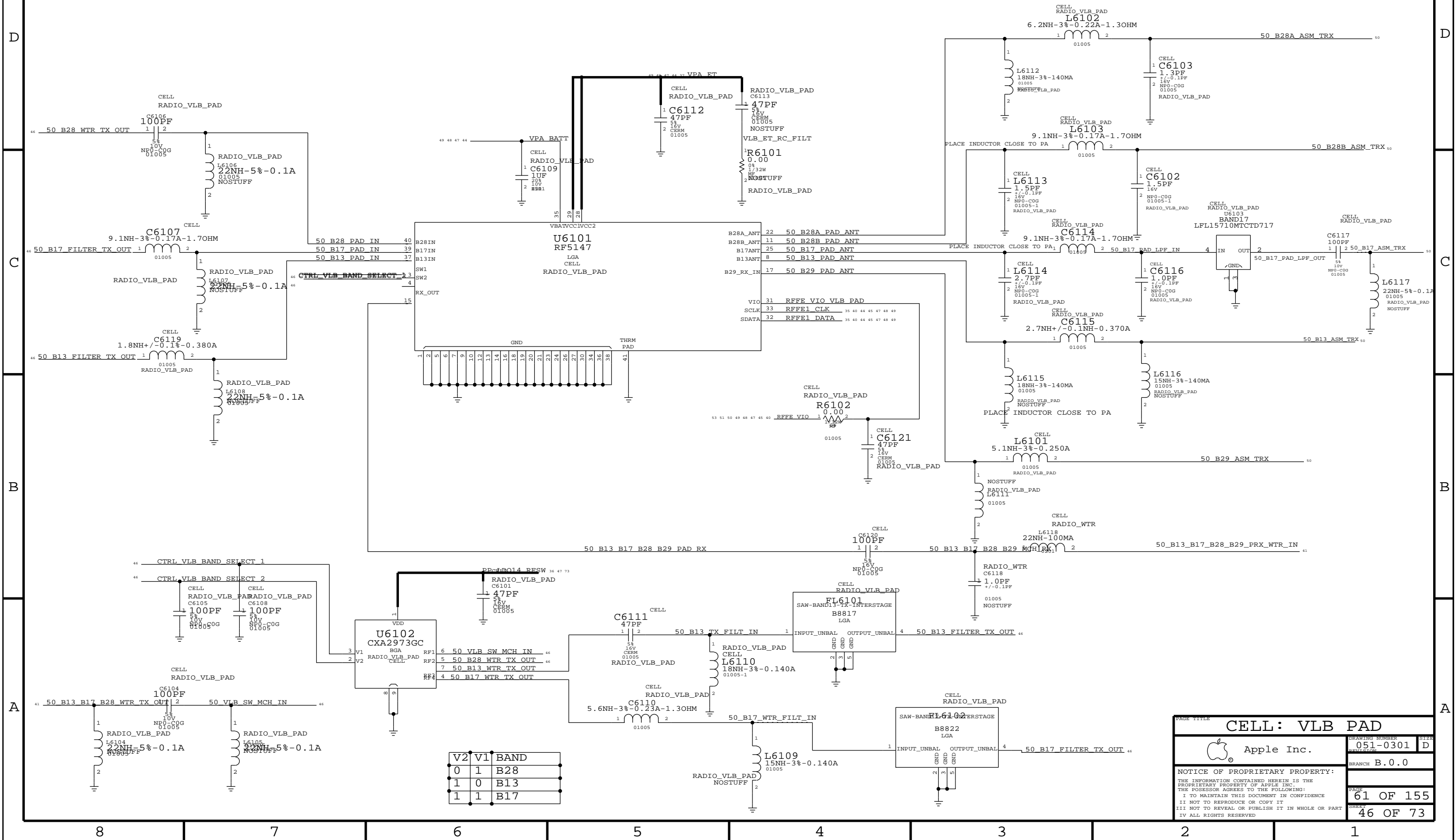
C1208
R1200
L1204
U1201

CHANGE TO VBATT!!!!



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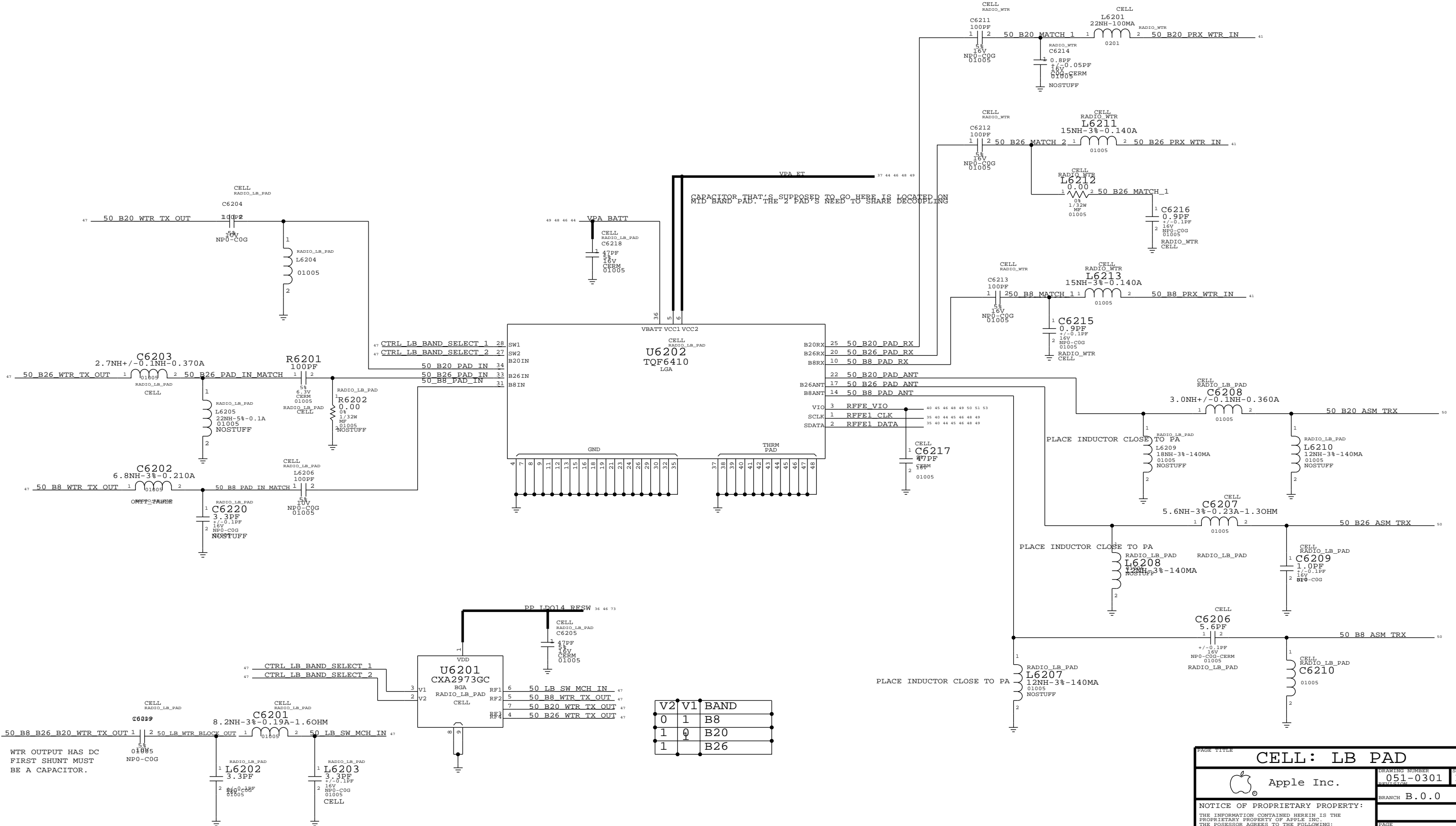
C1332
R1300
L4215_RF
U1304



LOW BAND PAD (B8, B26, B20)


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C4317_RF
R1400
L4316_RF
U1402



PAGE TITLE

CELL: LB PAD

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051-0301

SIZE
D

BRANCH
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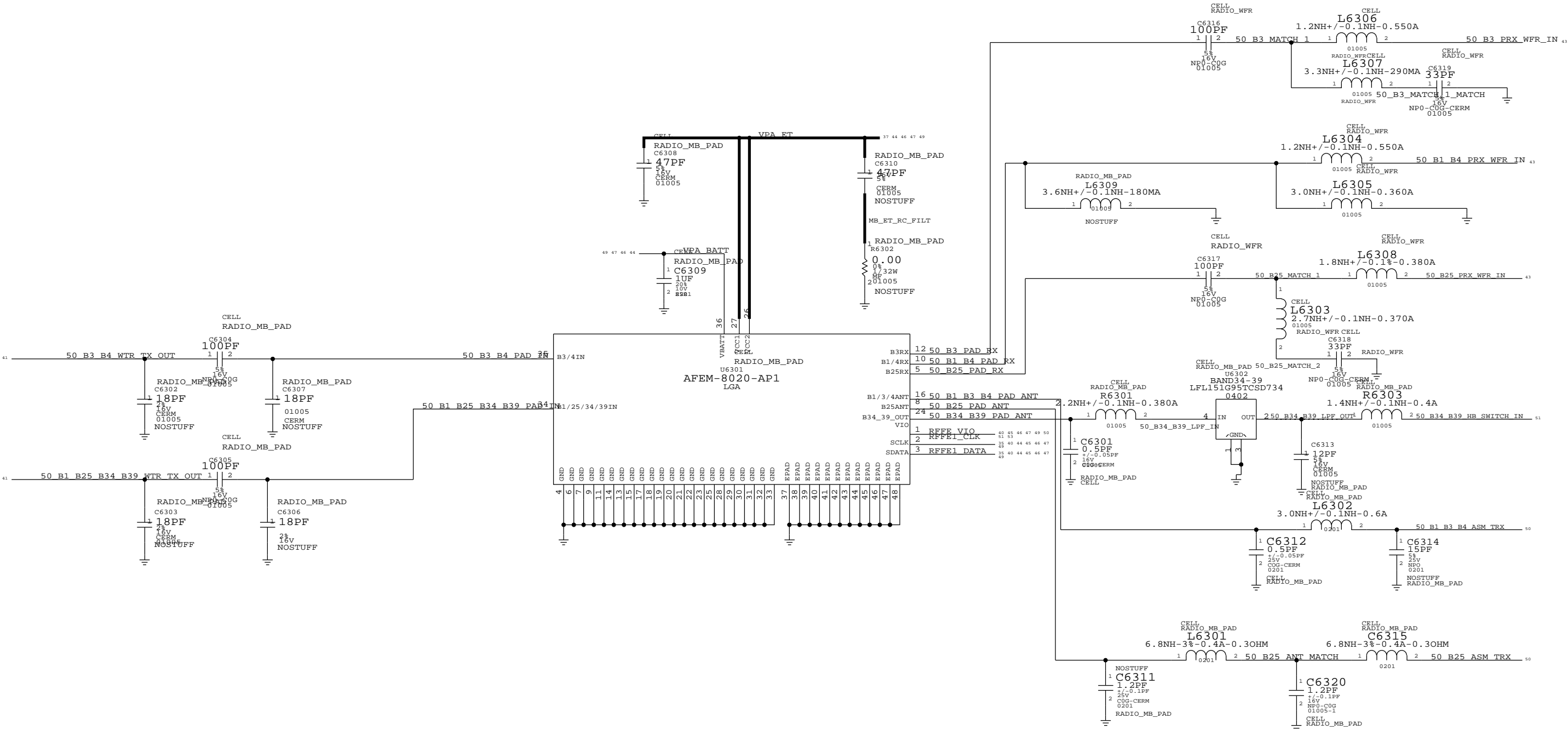
PAGE
62 OF 155

SHEET
47 OF 73

MID BAND PAD (B1, B25, B3, B4, B34, B39)

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C1510
R1500
L4409_RF
U1501

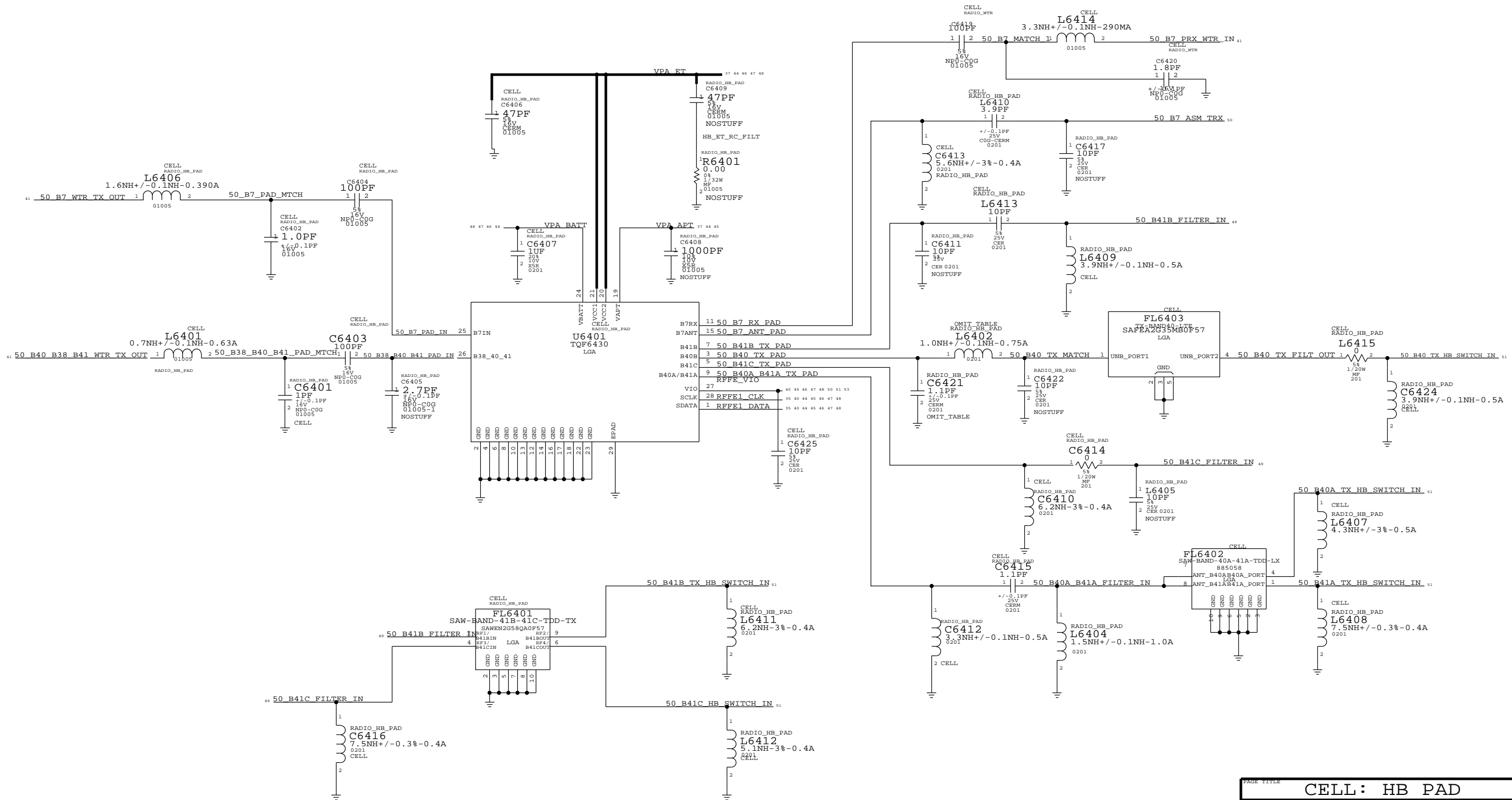



PAGE TITLE CELL: MB PAD		
Apple Inc.		DRAWING NUMBER 051-0301
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HIGH BAND PAD (B7, B38, B40, B41, XGP)

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C1614
R1600
L1616
U1601

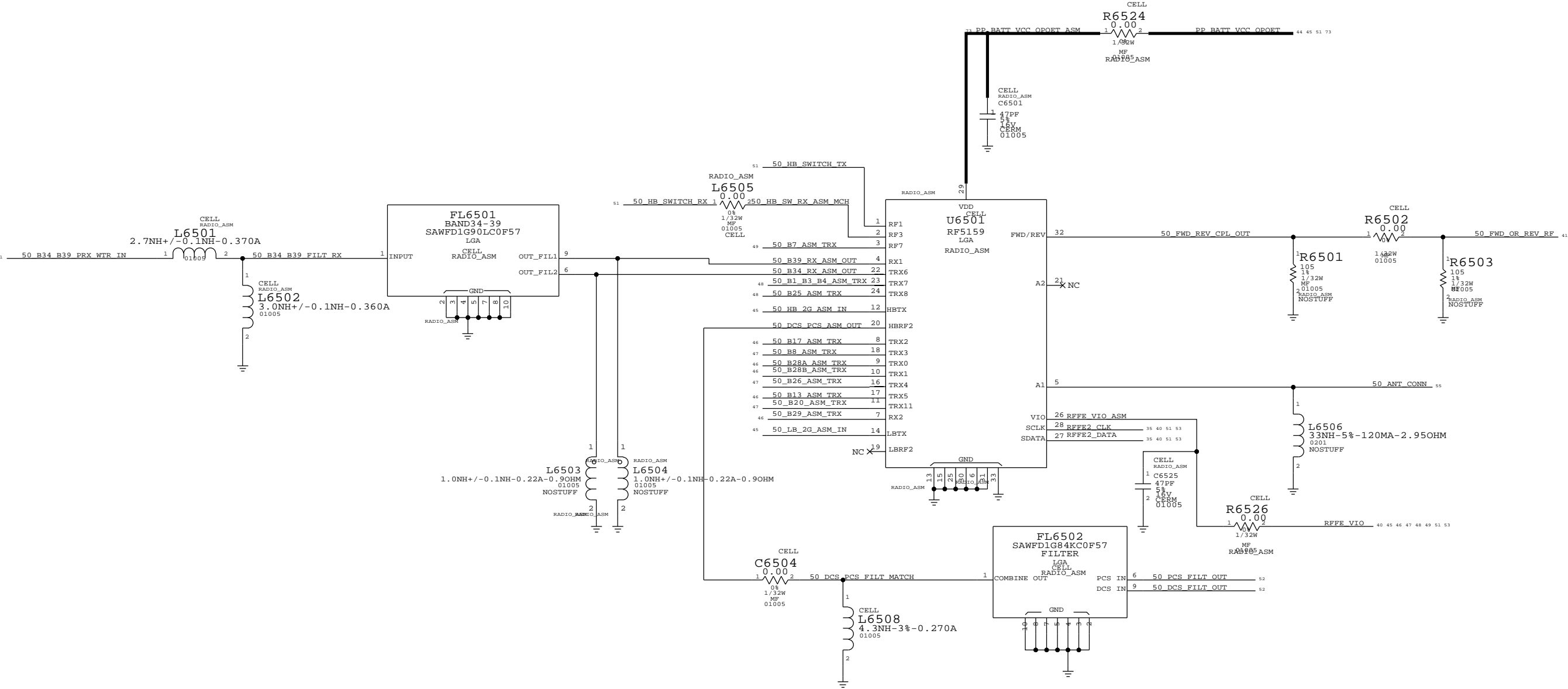


PAGE TITLE		
CELL: HB PAD		
 Apple Inc.	DRAWING NUMBER	051-0301
	SIZE	D
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	PAGE	64 OF 155
	SHEET	49 OF 73

ANTENNA SWITCH

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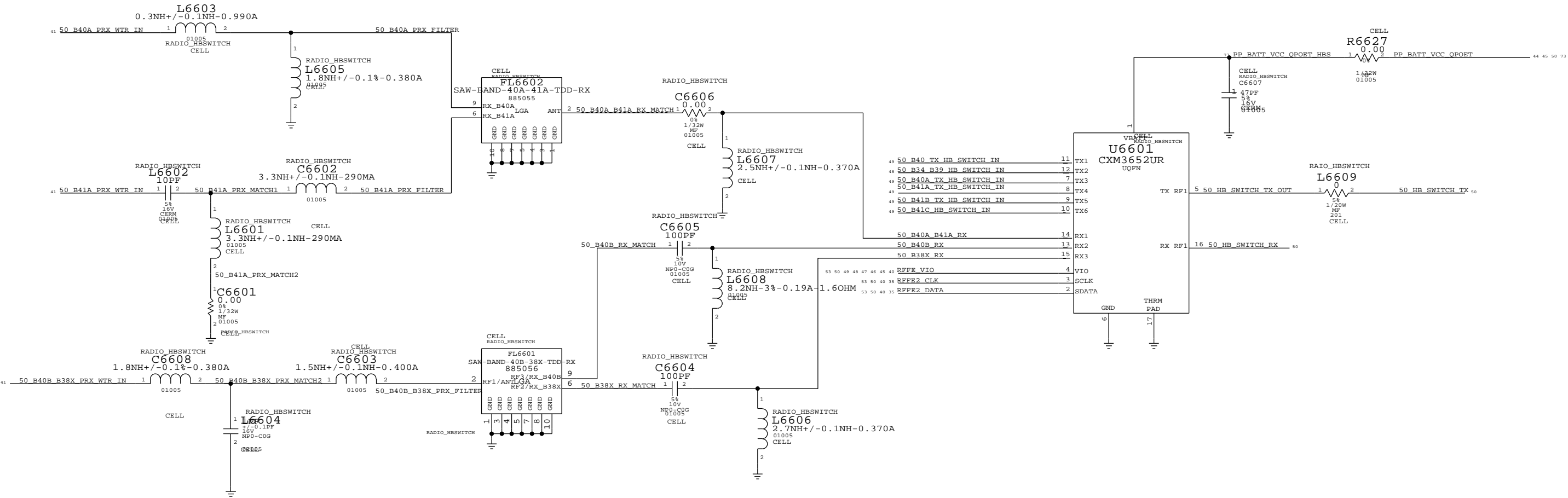
C1702
R1700
L4608_RF
U1702




CELL: ANTENNA SWITCH		
Apple Inc.	DRAWING NUMBER	051-0301
	SIZE	D
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	PAGE	65 OF 155
	SHEET	50 OF 73

HIGH BAND SWITCH

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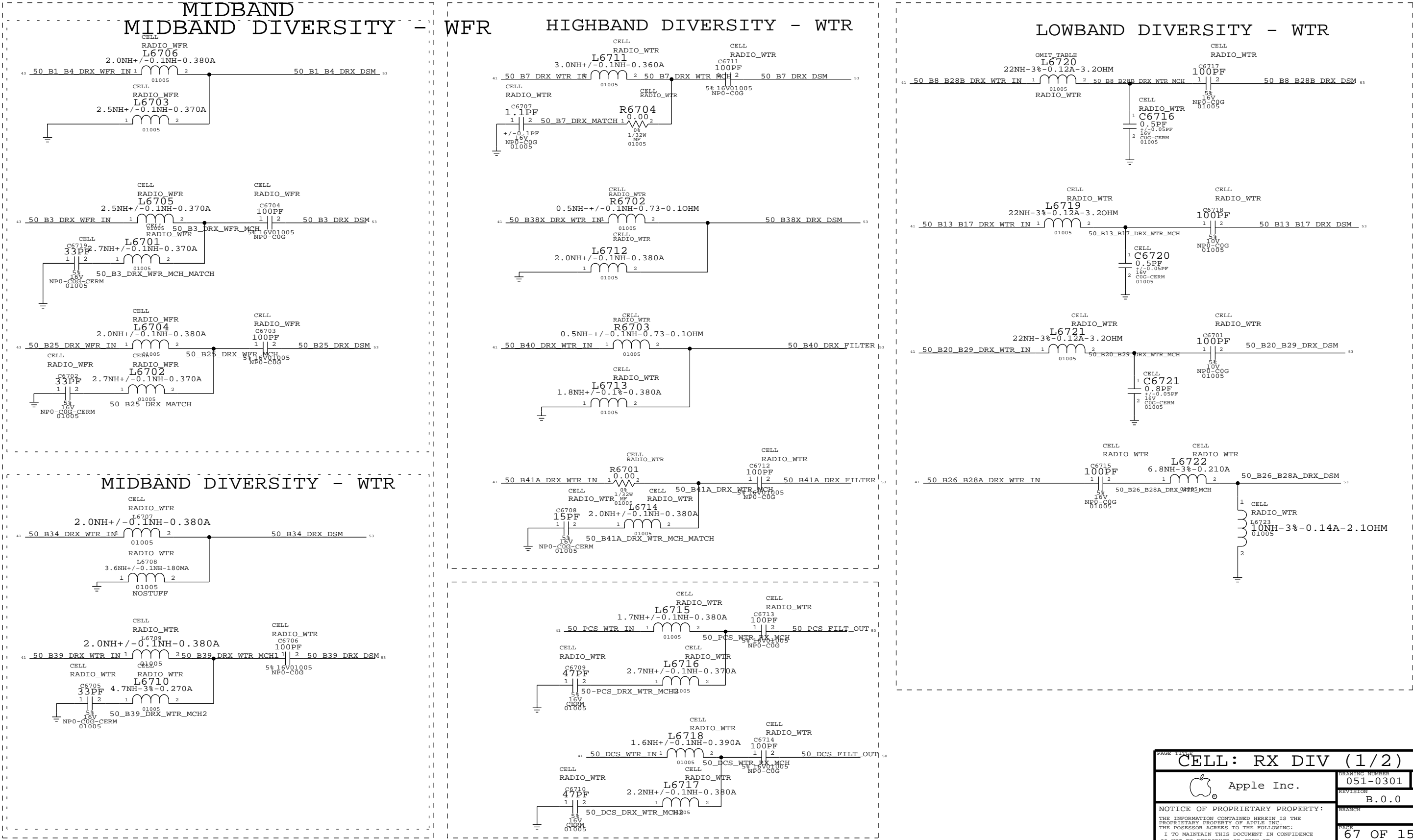


PAGE TITLE		
CELL: HB SWITCH		
 Apple Inc.	DRAWING NUMBER	051-0301
	SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH	B.0.0
	PAGE	00 OF 155
	SHEET	51 OF 73

RX DIVERSITY (1 OF 2)

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C4826_RF
R1800
L1829
U1801

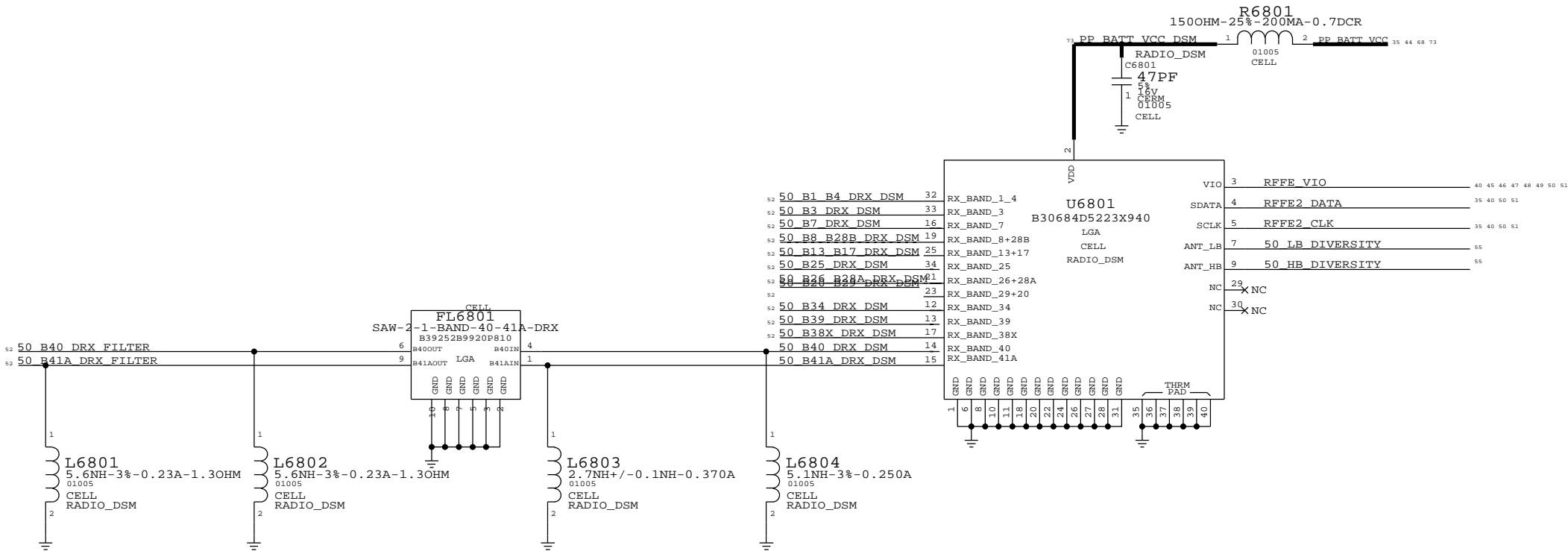


CELL: RX DIV (1/2)		
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PAGE 67 OF 155		SIZE D
SHEET 52 OF 73		

RX DIVERSITY (2 OF 2)

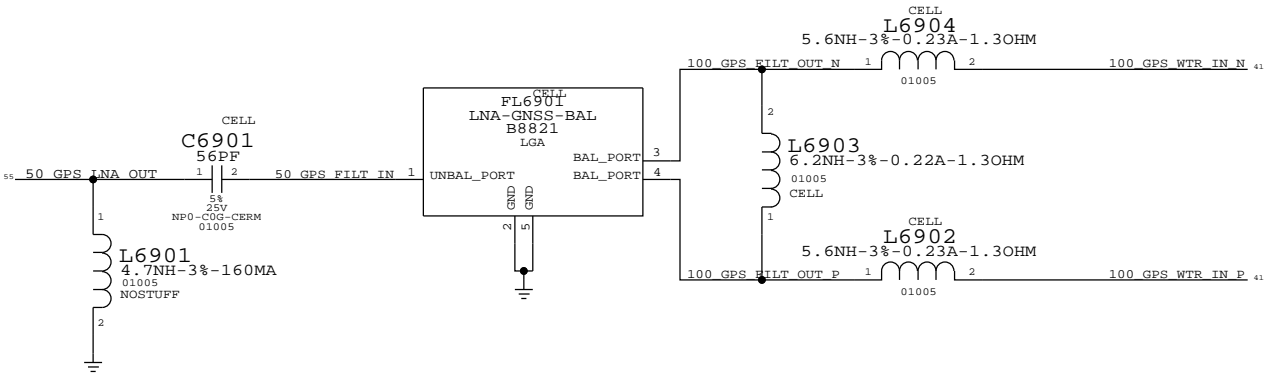
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C1900
R1900
L1900
U1901



GPS

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSES ONLY - NOT A CHANGE REQUEST.

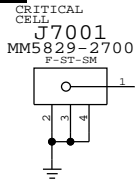


PAGE TITLE		
CELL: GPS		
 Apple Inc.	DRAWING NUMBER	051-0301
	SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH	B.0.0
	PAGE	69 OF 155
	SHEET	54 OF 73

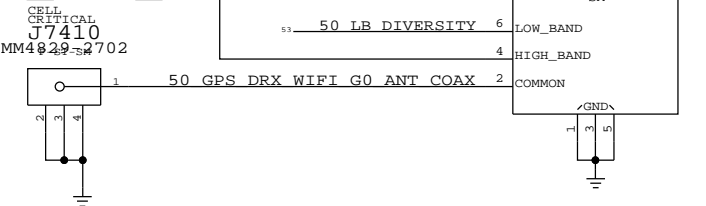
ANTENNA FEEDS AND GPS (J82)

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PRI_ANT COAX

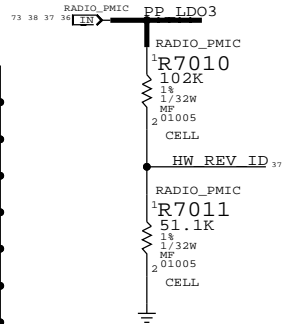


GPS_DRX_ANT



J82 HW_ID (MAPPING PG 52)
EVT


HW_REV_ID	R7010	R7011	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	PROTO0
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO1
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO2
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	PRE-EVT		
0.60V	102K	51.1K	EVT		
0.70V	82.5K	51.1K	DVT		



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0598		Y501	KDS XTAL, 19.2MHZ
197S0593	197S0598		Y501	NDK XTAL, 19.2MHZ

SYNC DATE=09/29/2014

CELL: ANT FEEDS & GPS (J82)

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D

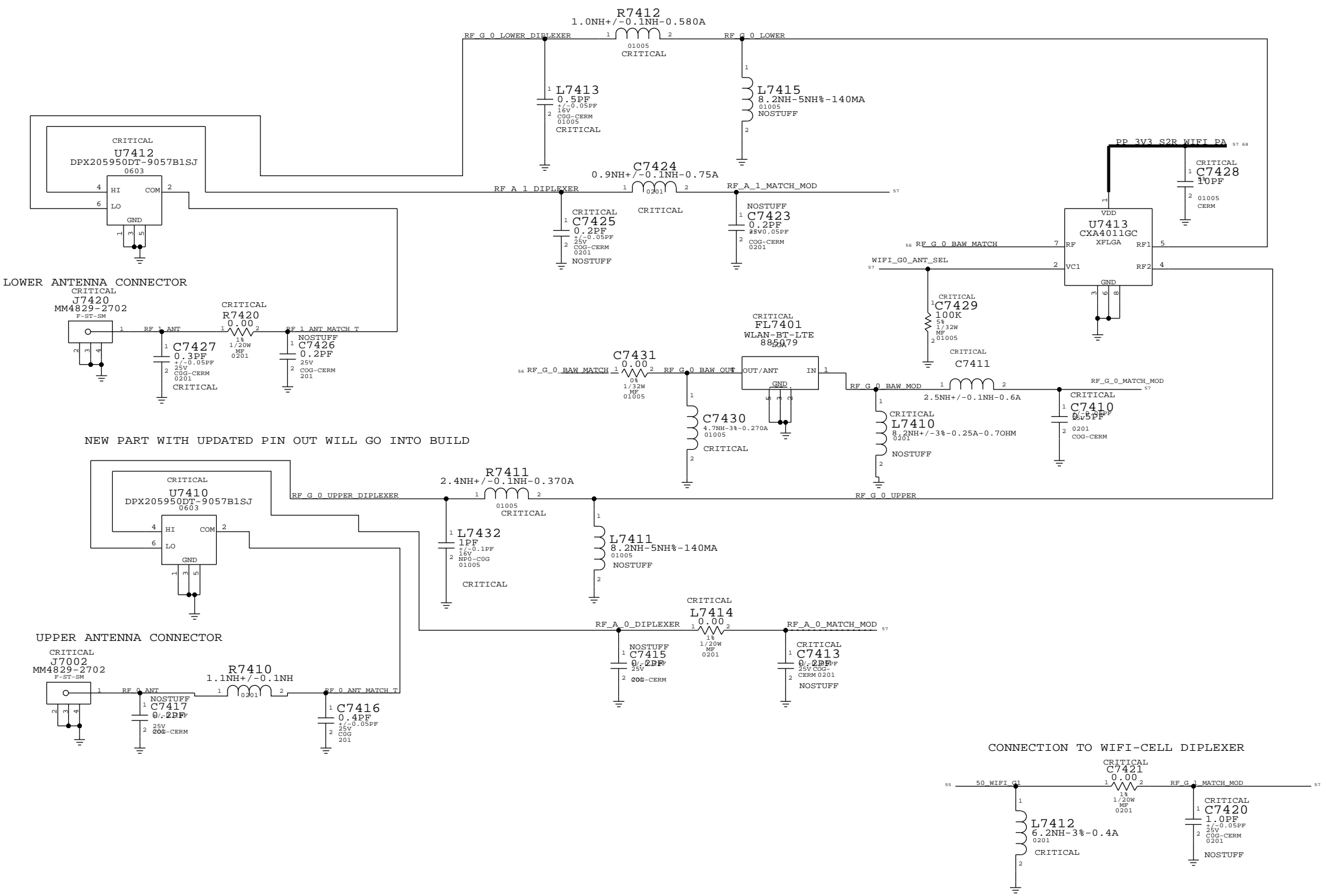
BRANCH
B.0.0

PAGE
70 OF 155

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WIFI/BT (2 OF 5)

WIFI/BT FRONT END FOR J82



NEW PART WITH UPDATED PIN OUT WILL GO INTO BUILD

CONNECTION TO WIFI-CELL DIPLEXER

PAGE TITLE	
WIFI/BT: J82 ANT INTERFACE	
Apple Inc.	
DRAWING NUMBER	051-0301
SIZE	D
BRANCH B.0.0	
PAGE 4 OF 155	
SHEET 56 OF 73	
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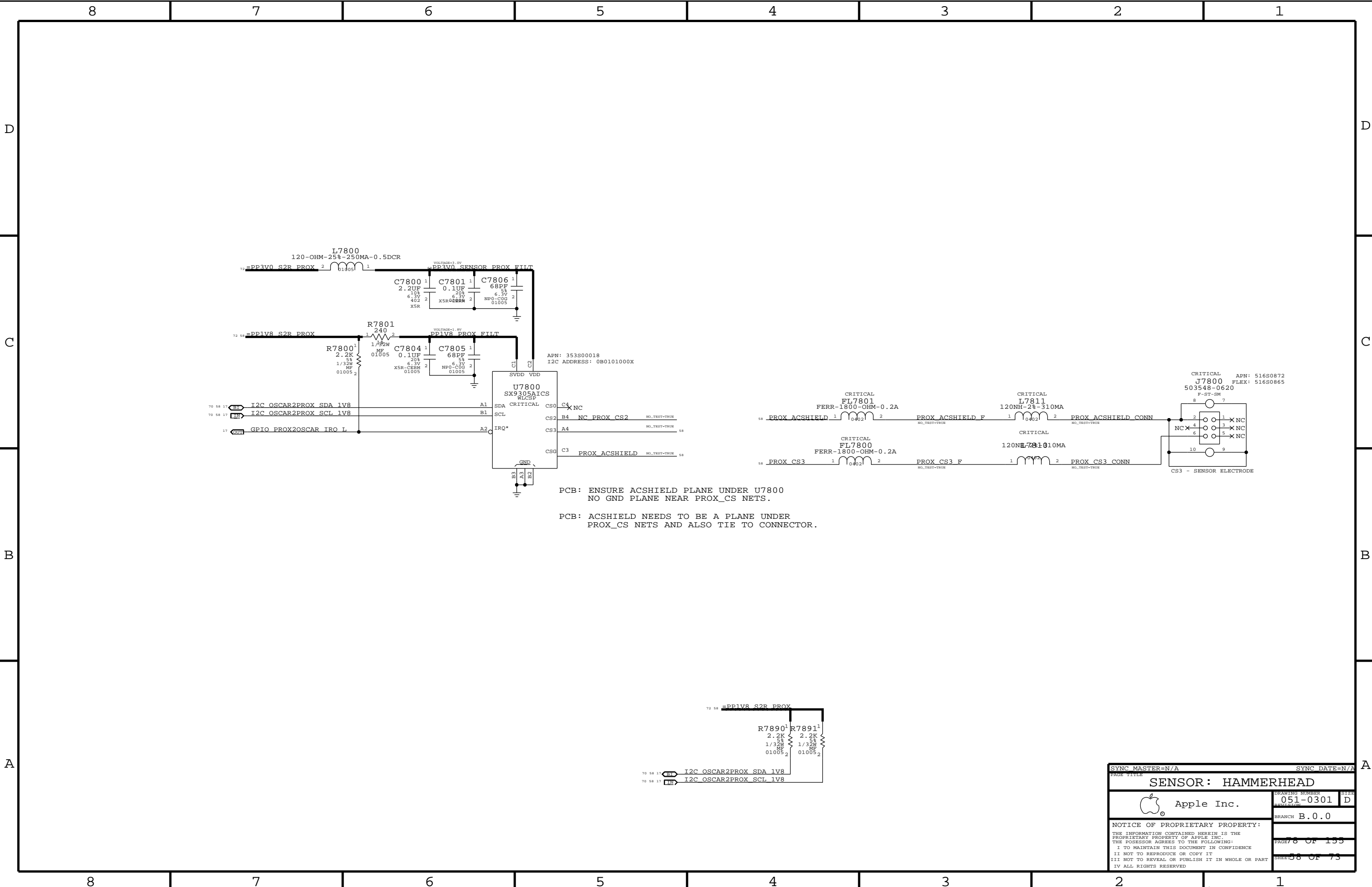
C

B



LAST UPDATED: 11/6/2013

SYNC MASTER-WIFI		SYNC DATE=09/29/2014	
PAGE TITLE			
WIFI/BT: WIFI/BT MODULE			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-0301	D
		REVISION	
		B.0.0	
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		75 OF 155	
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I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		57 OF 73	
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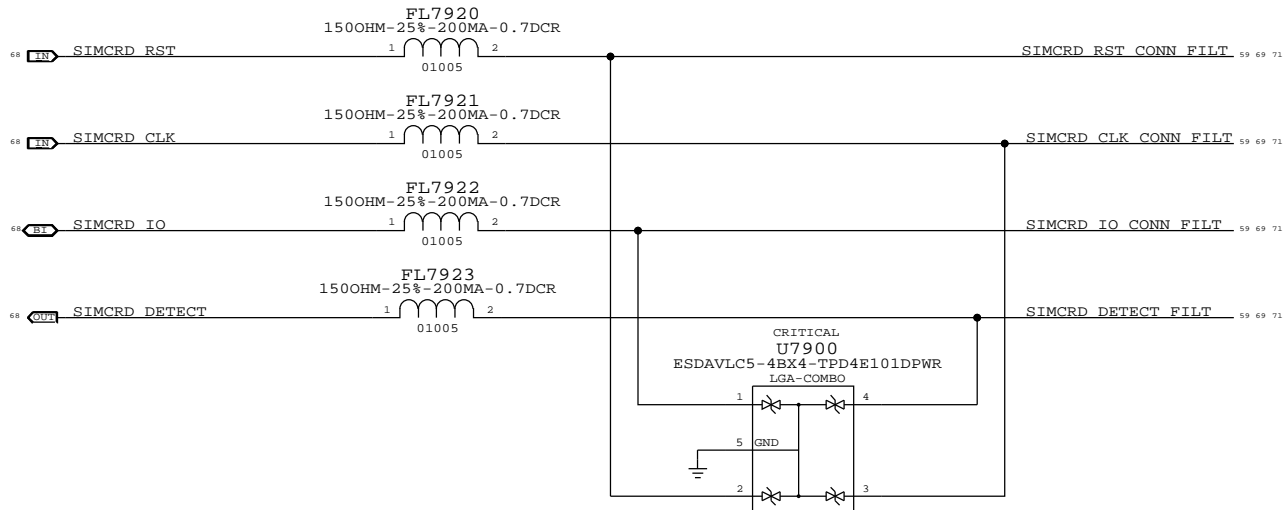
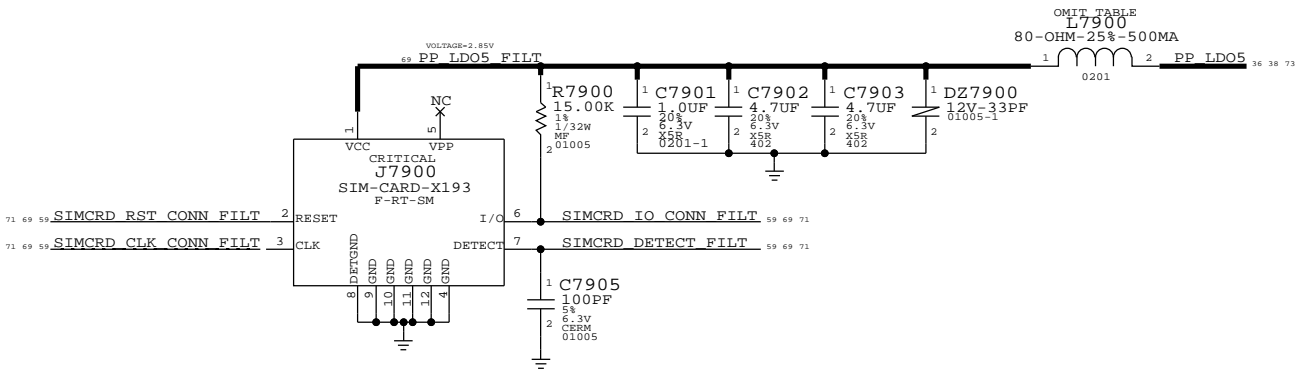
PCB: ENSURE ACSHIELD PLANE UNDER U7800
NO GND PLANE NEAR PROX_CS NETS.

PCB: ACSHIELD NEEDS TO BE A PLANE UNDER
PROX_CS NETS AND ALSO TIE TO CONNECTOR.

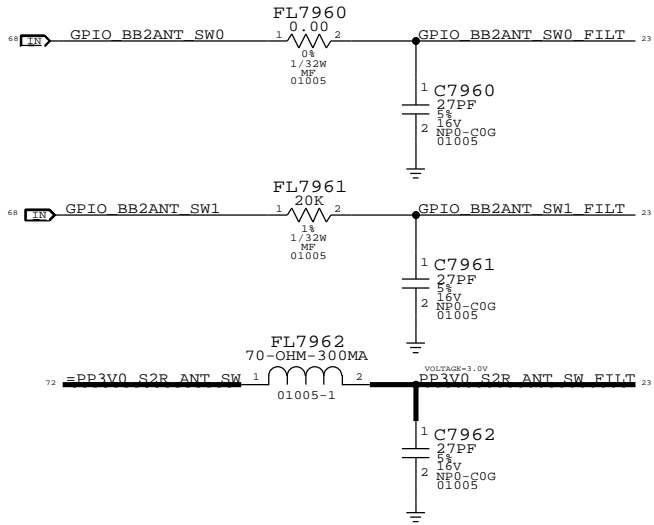
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SENSOR: HAMMERHEAD			
DRAWING NUMBER		SIZE	
051-0301		D	
BRANCH			
B.0.0			
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SIM CARD AND ANTENNA SWITCH FILTERS

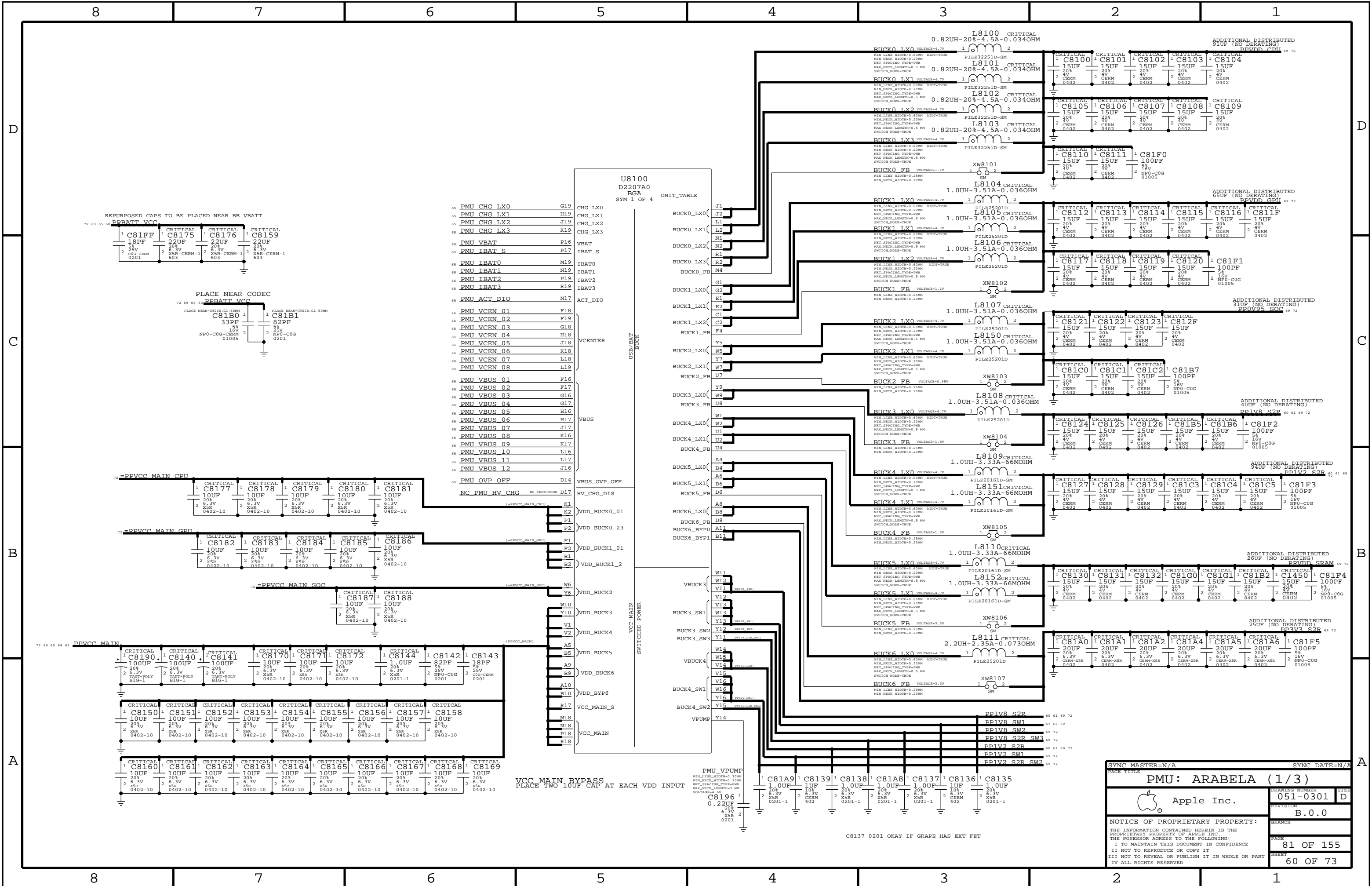
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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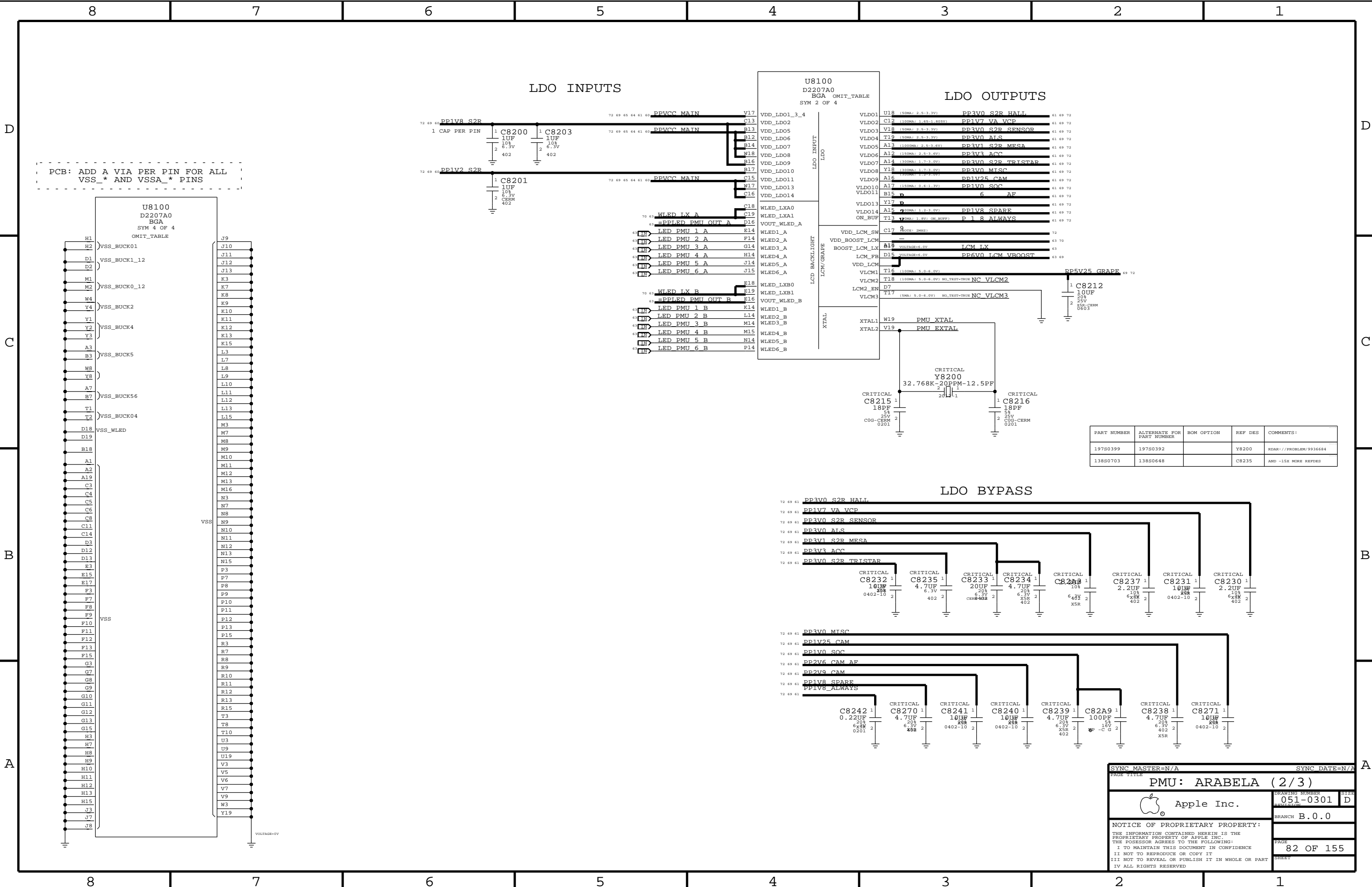


ANTENNA SWITCH FILTERS



SYNC MASTER=N/A		SYNC DATE=N/A	
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CELL: SIM AND ANT SW FILT			
 Apple Inc.		DRAWING NUMBER	051-0301
		REVISION	B.0.0
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		PAGE	79 OF 155
		SHEET	59 OF 73






PCB: ADD A VIA PER PIN FOR ALL
VSS_* AND VSSA_* PINS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR:///PROBLEM/9936684
138S0703	138S0648		C8235	AND -15X MORE REPDES

SYNC MASTER=N/A

SYNC DATE=N/A

PMU: ARABELA (2/3)

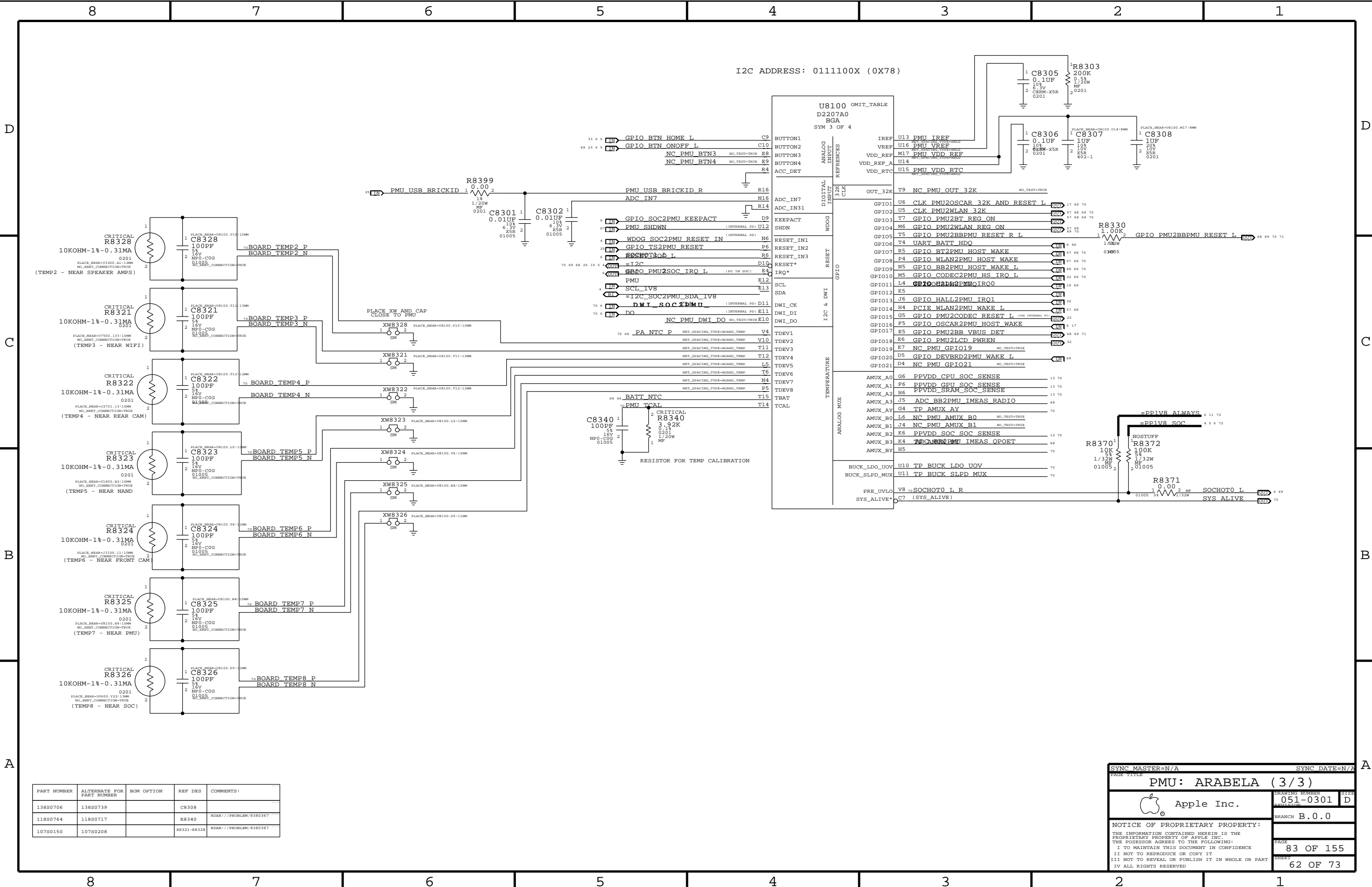
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051-0301
SIZE
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82 OF 155
SHEET



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C8308	
118S0764	118S0717		R8340	RDAR://PROBLEM/8380167
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380167

SYNC MASTER=N/A

SYNC DATE=N/A

PMU: ARABELA (3/3)

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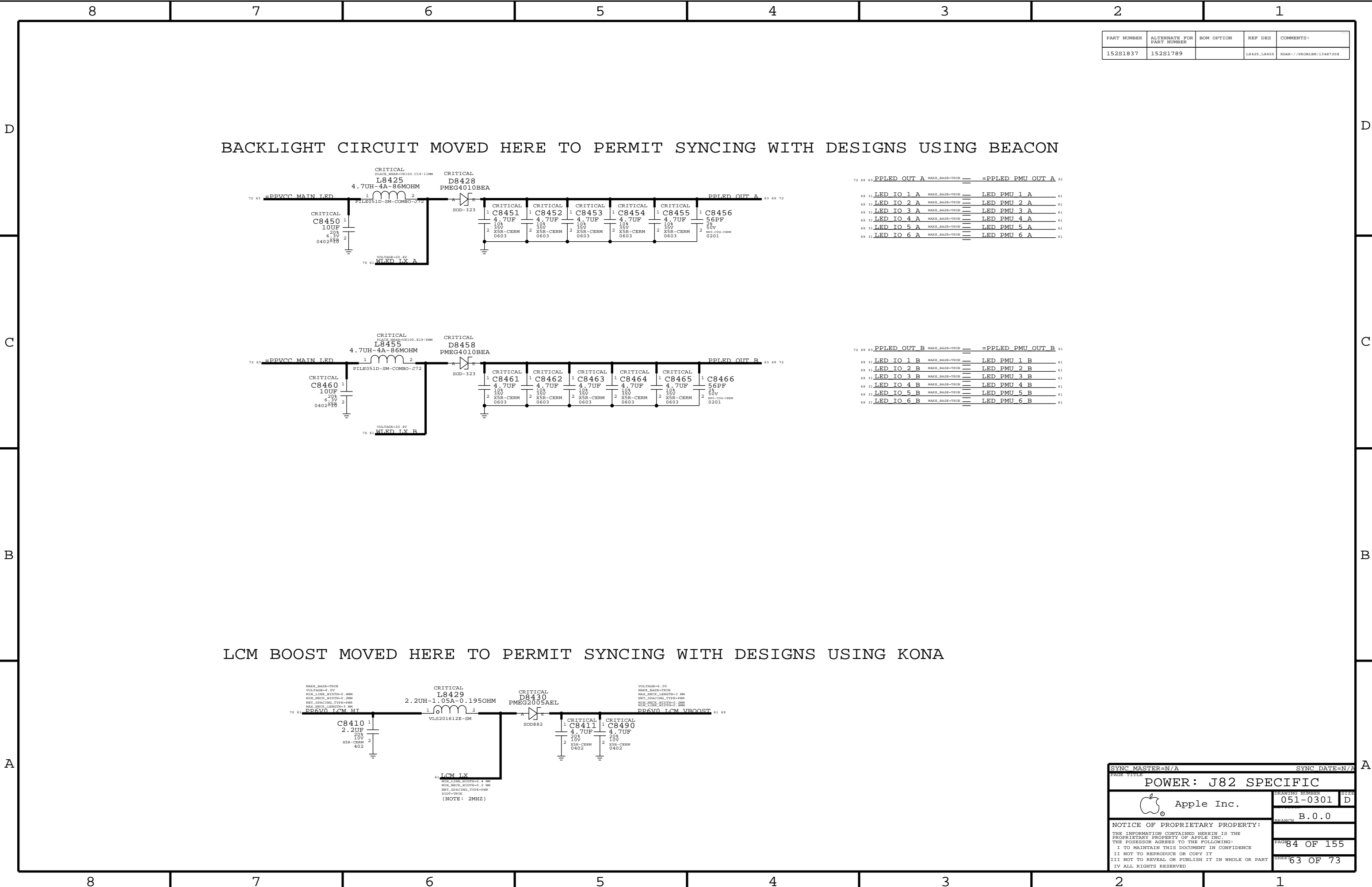
DRAWING NUMBER
051-0301

SIZE
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BRANCH
B.0.0

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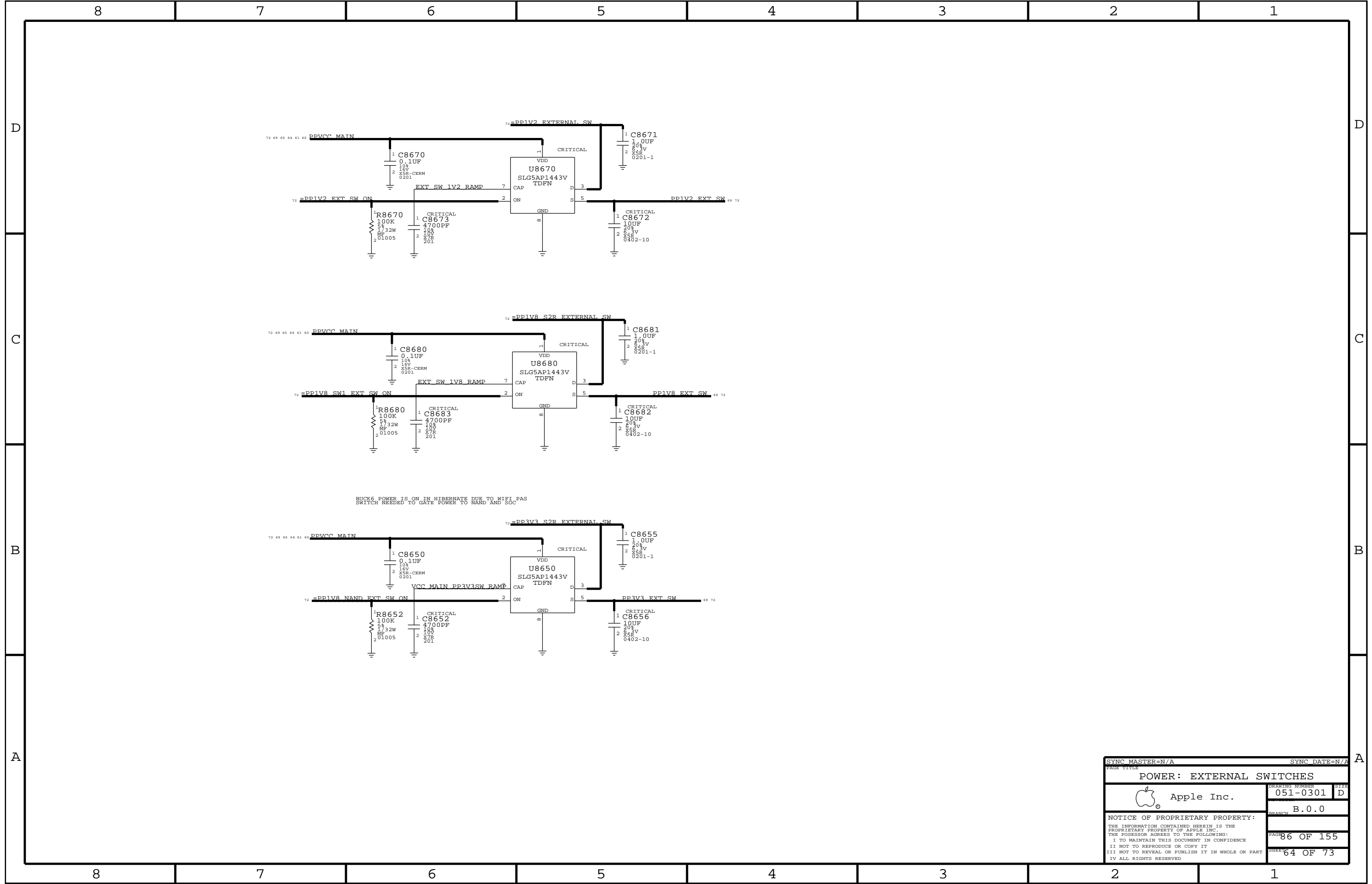


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152S1837	152S1789		L8425, L8455	EDAR: / / PROBLEM / 13487208

72	63	PPLED OUT A	MAKE_BASE=TRUE	=	PPLED PMU OUT A	61
69	31	LED TO 1 A	MAKE_BASE=TRUE	=	LED PMU 1 A	61
69	31	LED TO 2 A	MAKE_BASE=TRUE	=	LED PMU 2 A	61
69	31	LED TO 3 A	MAKE_BASE=TRUE	=	LED PMU 3 A	61
69	31	LED TO 4 A	MAKE_BASE=TRUE	=	LED PMU 4 A	61
69	31	LED TO 5 A	MAKE_BASE=TRUE	=	LED PMU 5 A	61
69	31	LED TO 6 A	MAKE_BASE=TRUE	=	LED PMU 6 A	61

72	69	63	PPLED OUT B	MAKE_BASE=TRUE	=	PPLED PMU OUT B	61
69	31	LED IO 1 B	MAKE_BASE=TRUE	=	LED PMU 1 B	61	
69	31	LED IO 2 B	MAKE_BASE=TRUE	=	LED PMU 2 B	61	
69	31	LED IO 3 B	MAKE_BASE=TRUE	=	LED PMU 3 B	61	
69	31	LED IO 4 B	MAKE_BASE=TRUE	=	LED PMU 4 B	61	
69	31	LED IO 5 B	MAKE_BASE=TRUE	=	LED PMU 5 B	61	
69	31	LED IO 6 B	MAKE_BASE=TRUE	=	LED PMU 6 B	61	

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
POWER: J82 SPECIFIC			
 Apple Inc.		DRAWING NUMBER	051-0301
		SIZE	D
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		PAGE	84 OF 155
		SHEET	63 OF 73



D

C

B

A

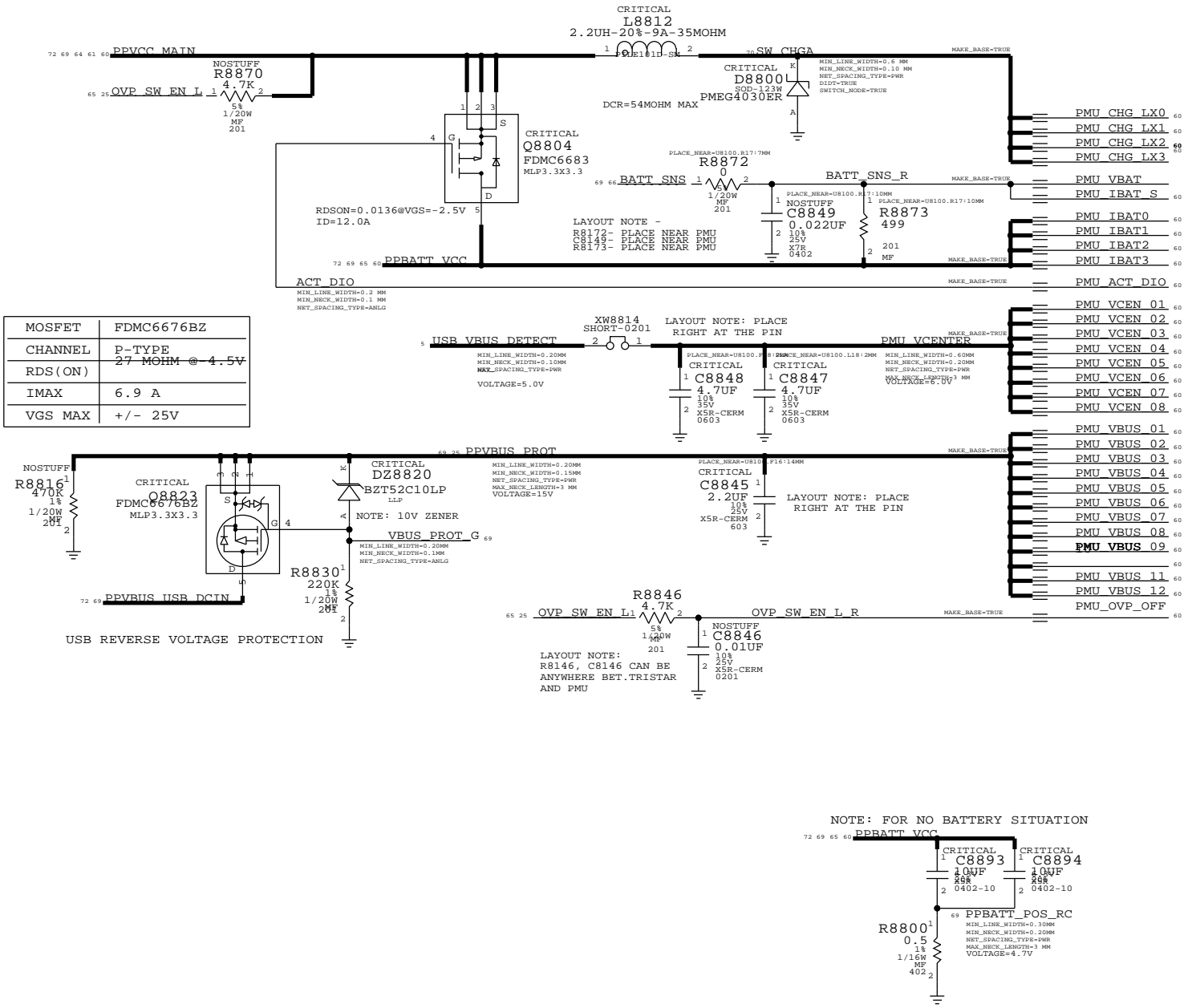
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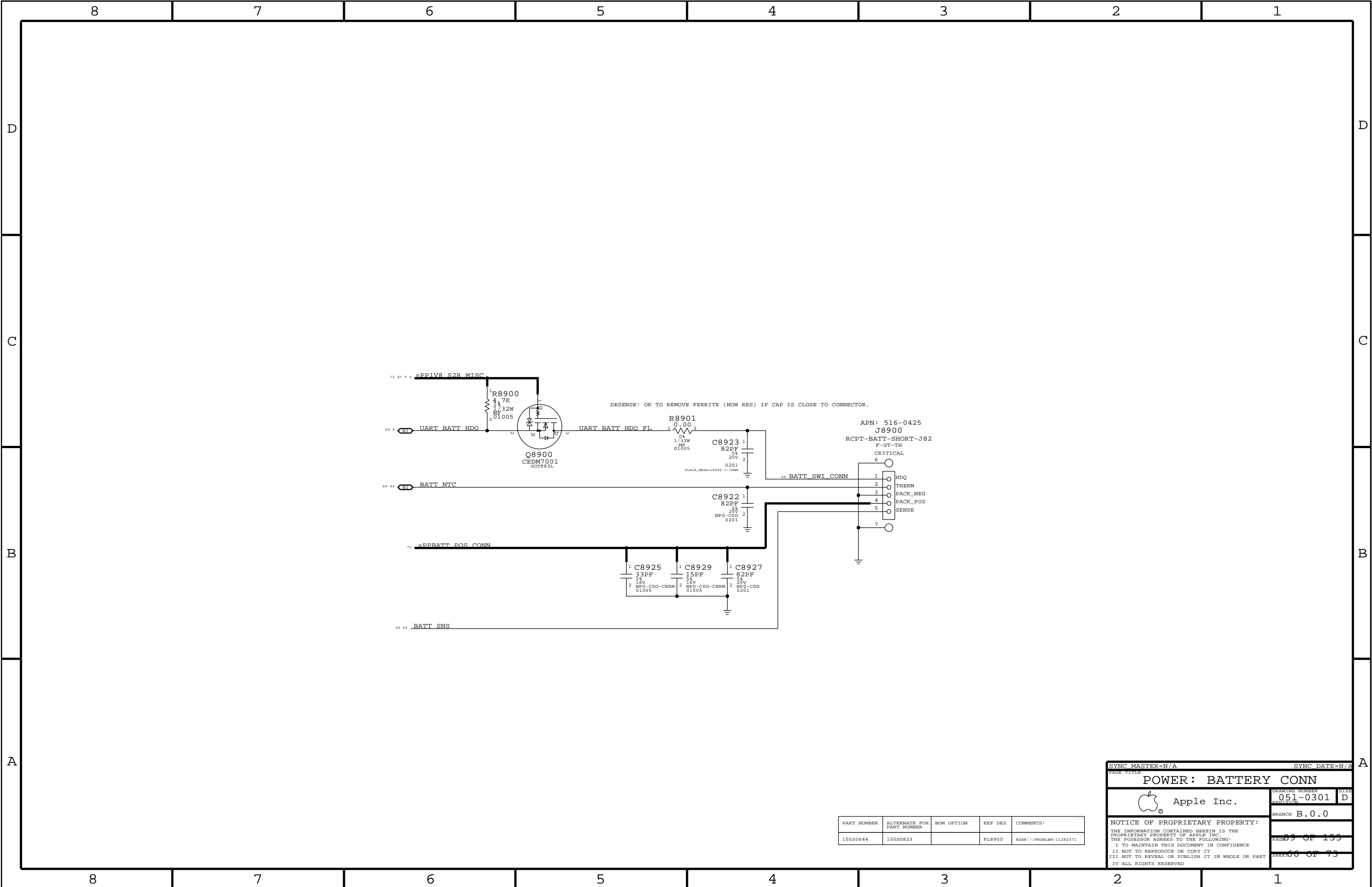
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A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1192	376S0929	?	Q8823	RDAR://PROBLEM/16073848



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
PMU: CHARGER BUCK			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-0301	D
		REVISION	
		BRANCH	B.0.0
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PAGE		88 OF 155	
SHEET			




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0823		FL8900	RDAR:///PROBLEM/11282371

SYNC MASTER=N/A

SYNC DATE=N/A

POWER: BATTERY CONN

 Apple Inc.

DRAWING NUMBER
051-0301
REVISION

SIZE
D

BRANCH
B.0.0

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DEBUG RESET ACCESS



CELLULAR AND WLAN/BT ALIASES

BASEBAND GPIO

71 69 6	IN	GPIO_SOC2BB_RADIO_ON_L	MAKE_BASE+TRUE	RADIO_ON_L	OUT	35 37
69 6	IN	GPIO_SOC2BB_RESET_L	MAKE_BASE+TRUE	BB_RST_L	OUT	35 37
69 6	OUT	GPIO_BB2SOC_RESET_DET_L	MAKE_BASE+TRUE	BB_RESET_DET_L	IN	35 37
70 69 62	IN	GPIO_PMU2BBPMU_RESET_L	MAKE_BASE+TRUE	RF_PMIC_RESET_L	OUT	35 37
71 6	IN	GPIO_SOC2BB_WAKE_MODEM	MAKE_BASE+TRUE	AP_WAKE_MODEM	OUT	40
70 69 62 25 10 5 4	OUT	RESET_SOC_L	MAKE_BASE+TRUE	RESET_1V8_L	IN	35
71 6	IN	GPIO_SOC2BB_COREDUMP	MAKE_BASE+TRUE	BB_CORE_DUMP	OUT	40
71 6	IN	GPIO_BB_IPC	MAKE_BASE+TRUE	BB_IPC_GPIO	IN	40
71 6	OUT	GPIO_BB2SOC_GPS_SYNC	MAKE_BASE+TRUE	BB_GPS_SYNC	IN	40
70 69 62	OUT	GPIO_BB2PMU_HOST_WAKE_L	MAKE_BASE+TRUE	BB_WAKE_HOST	IN	35 40

UART

71 25 6	OUT	UART_BB2SOC_TX	MAKE_BASE+TRUE	BB_UART_TXD	IN	35 40
71 25 6	IN	UART_SOC2BB_TX	MAKE_BASE+TRUE	BB_UART_RXD	OUT	35 40
71 6	OUT	UART_BB2SOC_RTS_L	MAKE_BASE+TRUE	BB_UART_RTS_L	IN	40
71 6	IN	UART_SOC2BB_RTS_L	MAKE_BASE+TRUE	BB_UART_CTS_L	OUT	40
71 17	IN	UART_OSCAR2BB_TX	MAKE_BASE+TRUE	BB_OTHER_RXD	OUT	40
71 17	OUT	UART_BB2OSCAR_TX	MAKE_BASE+TRUE	BB_OTHER_TXD	IN	40

HSIC

69 6	IN	HSIC_SOC2BB_HOST_RDY	MAKE_BASE+TRUE	BB_HOST_RDY	OUT	35 40
69 6	OUT	HSIC_BB2SOC_DEVICE_RDY	MAKE_BASE+TRUE	BB_DEVICE_RDY	IN	35 40
71 6	BT	HSIC_BB_DATA	MAKE_BASE+TRUE	50_BB_HSIC_DATA	BT	35 39
71 6	BT	HSIC_BB_STB	MAKE_BASE+TRUE	50_BB_HSIC_STROBE	BT	35 39

USB

71 69 62	IN	GPIO_PMU2BB_VBUS_DET	MAKE_BASE+TRUE	BB_USB_VBUS	OUT	35 39
71 26	BT	USB_BB_P	MAKE_BASE+TRUE	90_BB_USB_P	BT	35
71 26	BT	USB_BB_N	MAKE_BASE+TRUE	90_BB_USB_N	BT	35

SIM CARD

59	IN	SIMCRD_DETECT	MAKE_BASE+TRUE	BB_SIM_DETECT	OUT	39 40
59	OUT	SIMCRD_RST	MAKE_BASE+TRUE	BB_SIM_RESET	IN	40
59	OUT	SIMCRD_CLK	MAKE_BASE+TRUE	BB_SIM_CLK	IN	40
59	BT	SIMCRD_IO	MAKE_BASE+TRUE	BB_SIM_DATA	BT	40

ADC

62	OUT	ADC_BB2PMU_IMEAS_RADIO	MAKE_BASE+TRUE	RADIO_TO_PMU_ADC_IMEAS_RADIO	IN	35
62	OUT	ADC_BB2PMU_IMEAS_OPOET	MAKE_BASE+TRUE	RADIO_TO_PMU_ADC_IMEAS_OPOET	IN	44

POWER

72		=PPBATT_VCC_BB		PP_BATT_VCC		35 44 53 73
----	--	----------------	--	-------------	--	-------------

LOWER ANT CTRL

59	OUT	GPIO_BB2ANT_SW0	MAKE_BASE+TRUE	BB_ANTSW_GPIO0	IN	40
59	OUT	GPIO_BB2ANT_SW1	MAKE_BASE+TRUE	BB_ANTSW_GPIO1	IN	40

WLAN/BT GPIO

70 69 68 62 57	IN	CLK_PMU2WLAN_32K	MAKE_BASE+TRUE	CLK_PMU2WLAN_32K	OUT	57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2BT_REG_ON	MAKE_BASE+TRUE	GPIO_PMU2BT_REG_ON	OUT	57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2WLAN_REG_ON	MAKE_BASE+TRUE	GPIO_PMU2WLAN_REG_ON	OUT	57 62 68 69 70
70 68 57 9	IN	GPIO_SOC2BT_WAKE	MAKE_BASE+TRUE	GPIO_SOC2BT_WAKE	OUT	9 57 68 70
70 9	IN	GPIO_SOC2WLAN_WAKE	MAKE_BASE+TRUE	GPIO_SOC2WLAN_PCIE_DEV_WAKE	OUT	57
70 68 62 57	OUT	GPIO_BT2PMU_HOST_WAKE	MAKE_BASE+TRUE	GPIO_BT2PMU_HOST_WAKE	IN	57 62 68 70
70 68 62 57	OUT	GPIO_WLAN2PMU_HOST_WAKE	MAKE_BASE+TRUE	GPIO_WLAN2PMU_HOST_WAKE	IN	57 62 68 70

PCIE

70 9	IN	PCIE_SOC2WLAN_RESET_L	MAKE_BASE+TRUE	PCIE_SOC2WLAN_PERST	OUT	57
70 9	OUT	PCIE_WLAN2SOC_CLKREQ_L	MAKE_BASE+TRUE	PCIE_WLAN2SOC_CLKREQ	IN	57
68 62 57	OUT	PCIE_WLAN2PMU_WAKE_L	MAKE_BASE+TRUE	PCIE_WLAN2PMU_WAKE_L	IN	57 62 68
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_P	MAKE_BASE+TRUE	PCIE_SOC2WLAN_CLK_P	OUT	9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_N	MAKE_BASE+TRUE	PCIE_SOC2WLAN_CLK_N	OUT	9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_P	MAKE_BASE+TRUE	PCIE_SOC2WLAN_TX_P	OUT	9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_N	MAKE_BASE+TRUE	PCIE_SOC2WLAN_TX_N	OUT	9 57 68 70
70 9	OUT	PCIE_WLAN2SOC_TX_P	MAKE_BASE+TRUE	PCIE_WLAN2SOC_RX_P	IN	57
70 9	OUT	PCIE_WLAN2SOC_TX_N	MAKE_BASE+TRUE	PCIE_WLAN2SOC_RX_N	IN	57
70	OUT	PCIE_WLAN2SOC_TX_C_P	MAKE_BASE+TRUE	PCIE_TX_P	IN	57
70	OUT	PCIE_WLAN2SOC_TX_C_N	MAKE_BASE+TRUE	PCIE_TX_N	IN	57

TO KEEP PP NAMING CONSISTENT

UART

70 68 57 6	IN	UART_SOC2BT_TX	MAKE_BASE+TRUE	UART_SOC2BT_TX	OUT	6 57 68 70
70 68 57 6	IN	UART_SOC2BT_RTS_L	MAKE_BASE+TRUE	UART_SOC2BT_RTS_L	OUT	6 57 68 70
70 6	OUT	UART_BT2SOC_TX	MAKE_BASE+TRUE	UART_BT2SOC_RX	IN	57
70 6	OUT	UART_BT2SOC_RTS_L	MAKE_BASE+TRUE	UART_BT2SOC_CTS_L	IN	57
70 68 57 6	IN	UART_SOC2WLAN_TX	MAKE_BASE+TRUE	UART_SOC2WLAN_TX	OUT	6 57 68 70
70 68 57 6	IN	UART_SOC2WLAN_RTS_L	MAKE_BASE+TRUE	UART_SOC2WLAN_RTS_L	OUT	6 57 68 70
70 6	OUT	UART_WLAN2SOC_TX	MAKE_BASE+TRUE	UART_WLAN2SOC_RX	IN	57
70 6	OUT	UART_WLAN2SOC_RTS_L	MAKE_BASE+TRUE	UART_WLAN2SOC_CTS_L	IN	57

RESOLVES CKPLUS ERROR IN NAME

		TP_WL_UART_RX	MAKE_BASE+TRUE	WL_UART_RX		57
		TP_WL_UART_TX	MAKE_BASE+TRUE	WL_UART_TX		57

I2S

70 6	OUT	I2S_BT2SOC_DOUT	MAKE_BASE+TRUE	I2S_BT2SOC_DIN	IN	57
70 68 57 6	IN	I2S_SOC2BT_DOUT	MAKE_BASE+TRUE	I2S_SOC2BT_DOUT	OUT	6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_BCLK	MAKE_BASE+TRUE	I2S_SOC2BT_BCLK	OUT	6 57 68 70
70 68 57 6	IN	I2S_SOC2BT_LRCK	MAKE_BASE+TRUE	I2S_SOC2BT_LRCK	OUT	6 57 68 70

OSCAR CONTEXT

17	IN	GPIO_OSCAR2WLAN_CONTEXT_A	MAKE_BASE+TRUE	OSCAR2RADIO_CONTEXT_A	OUT	57 70
17	IN	GPIO_OSCAR2WLAN_CONTEXT_B	MAKE_BASE+TRUE	OSCAR2RADIO_CONTEXT_B	OUT	57 70

JTAG

70	IN	TP_JTAG_WLAN_TMS	MAKE_BASE+TRUE	JTAG_WLAN_TMS	IN	57
70	OUT	TP_JTAG_WLAN_TRST	MAKE_BASE+TRUE	JTAG_WLAN_TRST	IN	57

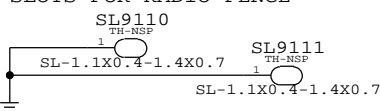
POWER

72		=PPVCC_MAIN_WLAN		PP_VCC_MAIN_WLAN		57
72		=PP3V3_S2R_WIFI_PA		PP_3V3_S2R_WIFI_PA		56 57
72		=PP1V8_S2R_VDDIO_WLAN_BT		PP_1V8_S2R_VDDIO_WLAN_BT		57 73

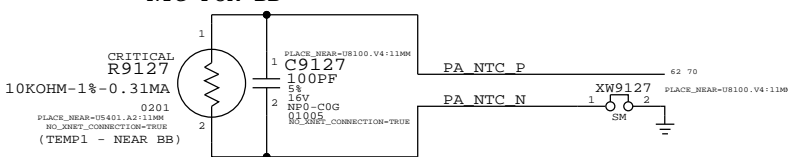
NO CONNECT

		NC_WLAN_GPIO3	NO_TEST+TRUE	MAKE_BASE+TRUE	BT_EXT_SYNC	OUT	57
		NC_WLAN_GPIO5	NO_TEST+TRUE	MAKE_BASE+TRUE	BT_EXT_CLK	OUT	57

SLOTS FOR RADIO FENCE



NTC FOR BB



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
ALIASES: BB/WLAN/BT			
Apple Inc.		DRAWING NUMBER 051-0301	SIZE D
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SMT TEST FIXTURE TP

POWER - BUCKS	
PPVDD CPU	FUNC_TEST=TRUE 60 72
PPVDD GPU	FUNC_TEST=TRUE 60 72
PPOV95 SOC	FUNC_TEST=TRUE 60 72
PP1V8 S2R	FUNC_TEST=TRUE 60 61 72
PP1V8 SW1	FUNC_TEST=TRUE 60 67 72
PP1V8 SW1 FOREHEAD	FUNC_TEST=TRUE 72
PP1V8 EXT SW	FUNC_TEST=TRUE 60 72
PP1V8 SW2	FUNC_TEST=TRUE 60 72
PP1V8 GRAPE EXT SW	FUNC_TEST=TRUE 30 72
PP1V8 S2R SW3	FUNC_TEST=TRUE 60 72
PP1V2 S2R	FUNC_TEST=TRUE 60 61 72
PP1V2 SW1	FUNC_TEST=TRUE 64 72
PP1V2 EXT SW	FUNC_TEST=TRUE 60 72
PP1V2 S2R SW2	FUNC_TEST=TRUE 60 72
PPVDD SRAM	FUNC_TEST=TRUE 60 72
PP3V3 S2R	FUNC_TEST=TRUE 60 72
PP3V3 EXT SW	FUNC_TEST=TRUE 64 72

POWER - LDOS	
PP1V7 VA VCP	FUNC_TEST=TRUE 61 72
PP3V0 S2R SENSOR	FUNC_TEST=TRUE 61 72
PP3V0 ALS	FUNC_TEST=TRUE 61 72
PP3V3 ACC	FUNC_TEST=TRUE 61 72
PP3V0 S2R TRISTAR	FUNC_TEST=TRUE 61 72
PP3V1 S2R MESA	FUNC_TEST=TRUE 61 72
PP1V0	FUNC_TEST=TRUE 61 72
PP1V8 SPARE	FUNC_TEST=TRUE 61 72
PP3V0 S2R HALL	FUNC_TEST=TRUE 61 72
PP3V0 MISC	FUNC_TEST=TRUE 61 72
PP1V25 CAM	FUNC_TEST=TRUE 61 72
PP2V6 CAM AF	FUNC_TEST=TRUE 61 72
PP2V9 CAM	FUNC_TEST=TRUE 61 72

POWER - OTHER	
PP1V8 ALWAYS	FUNC_TEST=TRUE 61 72
PPBATT VCC	FUNC_TEST=TRUE 60 65 69 72
PPLED OUT A	FUNC_TEST=TRUE 63 72
PPLED OUT B	FUNC_TEST=TRUE 63 72
PP3V25 GRAPE	FUNC_TEST=TRUE 61 72
PP1V8 XTAL	FUNC_TEST=TRUE 11
PPVCC MAIN	FUNC_TEST=TRUE 60 61 64 65 72
PPBATT POS RC	FUNC_TEST=TRUE 61 72
PP6V0 LCM VBOOST	FUNC_TEST=TRUE 61 63
PPVBUS USB DCIN	FUNC_TEST=TRUE 65 72
PPVBUS PROT	FUNC_TEST=TRUE 25 65
VBUS PROT G	FUNC_TEST=TRUE 65

POWER - CAMERA (FRONT)	
PP1V2 CAM FRONT FILT	FUNC_TEST=TRUE 20 21
PP1V8 CAM FRONT FILT	FUNC_TEST=TRUE 20 21
PP2V9 AVDD CAM FRONT FILT	FUNC_TEST=TRUE 20 21

POWER - CAMERA (REAR)	
PP1V25 CAM REAR FILT	FUNC_TEST=TRUE 20 21
PP1V8 CAM REAR FILT	FUNC_TEST=TRUE 20 21
PP2V6 CAM REAR AF FILT	FUNC_TEST=TRUE 20 21
PP2V9 AVDD CAM REAR FILT	FUNC_TEST=TRUE 20 21

POWER - AUDIO	
PP1V8 DMIC MIC FILT	FUNC_TEST=TRUE 23
PP1V8 DMIC BTN FILT	FUNC_TEST=TRUE 28
PP1V7 VCP	FUNC_TEST=TRUE 24
PPVBOOST R	FUNC_TEST=TRUE 24
PPVBOOST L	FUNC_TEST=TRUE 24

POWER - SENSORS	
PP1V8 COMPASS	FUNC_TEST=TRUE 18
PP1V8 PHOS FILT	FUNC_TEST=TRUE 18
PP1V8 OSCAR FILT	FUNC_TEST=TRUE 17
PP1V2 OSCAR FILT	FUNC_TEST=TRUE 17
PP3V0 GYRO FILT	FUNC_TEST=TRUE 18
PP3V0 SENSOR PROX FILT	FUNC_TEST=TRUE 58

POWER - DISPLAY	
PPVCC MAIN LCD SW CONN	FUNC_TEST=TRUE 31 32
PPVCC MAIN LCD SW	FUNC_TEST=TRUE 32

POWER - MESA	
PP1V825 S2R MESA FILT	FUNC_TEST=TRUE 31 33
PP3V1 S2R MESA FILT	FUNC_TEST=TRUE 31 33
PP11V3 MESA FILT	FUNC_TEST=TRUE 31 33

POWER - GRAPE	
PPVDD STINGER BOOST	FUNC_TEST=TRUE 29

POWER - BACKLIGHT	
PPLED BACK REG A	FUNC_TEST=TRUE 31 32
LED IO 1 A	FUNC_TEST=TRUE 31 63
LED IO 2 A	FUNC_TEST=TRUE 31 63
LED IO 3 A	FUNC_TEST=TRUE 31 63
LED IO 4 A	FUNC_TEST=TRUE 31 63
LED IO 5 A	FUNC_TEST=TRUE 31 63
LED IO 6 A	FUNC_TEST=TRUE 31 63
PPLED BACK REG B	FUNC_TEST=TRUE 31 32
LED IO 1 B	FUNC_TEST=TRUE 31 63
LED IO 2 B	FUNC_TEST=TRUE 31 63
LED IO 3 B	FUNC_TEST=TRUE 31 63
LED IO 4 B	FUNC_TEST=TRUE 31 63
LED IO 5 B	FUNC_TEST=TRUE 31 63
LED IO 6 B	FUNC_TEST=TRUE 31 63

SOC - JTAG/RESET	
JTAG SOC SEL	FUNC_TEST=TRUE 4 5
JTAG SOC TCK	FUNC_TEST=TRUE 5 25
JTAG SOC TDI	FUNC_TEST=TRUE 5
JTAG SOC TMS	FUNC_TEST=TRUE 5 25
TP JTAG SOC TRST L	FUNC_TEST=TRUE 5 5
TP JTAG SOC TDO	FUNC_TEST=TRUE 4 5
SOC TESTMODE	FUNC_TEST=TRUE 4 5
RESET SOC L	FUNC_TEST=TRUE 4 5 10 25 62 68 70
GPIO FORCE DFU	FUNC_TEST=TRUE 6 67

SOC - UART	
UART SOC2DEBUG TX	FUNC_TEST=TRUE 6 25
UART DEBUG2SOC TX	FUNC_TEST=TRUE 6 25

SOC - USB	
USB SOC N	FUNC_TEST=TRUE 5 25
USB SOC P	FUNC_TEST=TRUE 5 25

E75 ACC DET CONN L	
PPVBUS E75 USB CONN	FUNC_TEST=TRUE 26 27
PPPOUT E75 ACC ID1 CONN	FUNC_TEST=TRUE 26 27 68
PPPOUT E75 ACC ID2 CONN	FUNC_TEST=TRUE 26 27
E75 DPAIR1 CONN N	FUNC_TEST=TRUE 26 27
E75 DPAIR1 CONN P	FUNC_TEST=TRUE 26 27
E75 DPAIR2 CONN N	FUNC_TEST=TRUE 26 27
E75 DPAIR2 CONN P	FUNC_TEST=TRUE 26 27

AUDIO - HEADPHONE	
CONN HP HEADSET DET FILT	FUNC_TEST=TRUE 22 23
CONN HP HS3 FILT	FUNC_TEST=TRUE 22 23
CONN HP HS3 REF FILT	FUNC_TEST=TRUE 22 23
CONN HP HS4 FILT	FUNC_TEST=TRUE 22 23
CONN HP HS4 REF FILT	FUNC_TEST=TRUE 22 23
CONN HP LEFT FILT	FUNC_TEST=TRUE 22 23
CONN HP RIGHT FILT	FUNC_TEST=TRUE 22 23
GPIO SOC2AJ HS3 SHUNT EN FILT	FUNC_TEST=TRUE 23
GPIO SOC2AJ HS4 SHUNT EN FILT	FUNC_TEST=TRUE 23

AUDIO - SPEAKER AMPS	
SPKRAMP L OUT N	FUNC_TEST=TRUE 24 27 70
SPKRAMP L OUT P	FUNC_TEST=TRUE 24 27 70
SPKRAMP R OUT N	FUNC_TEST=TRUE 24 27 70
SPKRAMP R OUT P	FUNC_TEST=TRUE 24 27 70

AUDIO - CODEC	
AIN3P	FUNC_TEST=TRUE 22
AIN3N	FUNC_TEST=TRUE 22
GPIO CODEC2PMU HS IRQ L	FUNC_TEST=TRUE 22 62 70
GND AUDIO CODEC	FUNC_TEST=TRUE 22
MIKEY TS P	FUNC_TEST=TRUE 22 25
MIKEY TS N	FUNC_TEST=TRUE 22 25

AUDIO - DIGITAL MICS	
DMIC MIC SCLK	FUNC_TEST=TRUE 22 23
DMIC BTN SCLK	FUNC_TEST=TRUE 22 28

BUTTONS	
GPIO BTN HOME CONN L	FUNC_TEST=TRUE 31 33
GPIO BTN ONOFF L	FUNC_TEST=TRUE 5 6 23 62
GPIO BTN VOL UP L FILT	FUNC_TEST=TRUE 28
GPIO BTN VOL DOWN L FILT	FUNC_TEST=TRUE 28

NAND	
ANC0 CE0 L	FUNC_TEST=TRUE 7 16 70
ANC1 CE0 L	FUNC_TEST=TRUE 7 16 70

BATTERY	
BATT SWI CONN	FUNC_TEST=TRUE 66
BATT NTC	FUNC_TEST=TRUE 62 66
BATT SNS	FUNC_TEST=TRUE 65 66

GRAPE	
CLK_SOC2GRAPE 32K	FUNC_TEST=TRUE 9 30 70

BASEBAND	
BOUNDARY SCAN EN	FUNC_TEST=TRUE 35 39
GPIO PMU2BBPMU RESET L	FUNC_TEST=TRUE 62 68 70 71
GPIO SOC2BB RADIO ON L	FUNC_TEST=TRUE 6 68 71
HSIC SOC2BB HOST RDY	FUNC_TEST=TRUE 6 68
GPIO BB2SOC RESET DET L	FUNC_TEST=TRUE 6 68
HSIC BB2SOC DEVICE RDY	FUNC_TEST=TRUE 6 68
GPIO SOC2BB RESET L	FUNC_TEST=TRUE 6 68
GPIO PMU2BB VBUS DET	FUNC_TEST=TRUE 62 68 71
GPIO BB2PMU HOST WAKE L	FUNC_TEST=TRUE 62 68 70

BASEBAND - POWER	
PP LDO6	FUNC_TEST=TRUE 35 36 71 73
PP LDO13	FUNC_TEST=TRUE 36 38 55 73
VREG SMP51 OV90	FUNC_TEST=TRUE 36 38
VREG SMP53 OV95	FUNC_TEST=TRUE 36 73

BASEBAND - SIM CARD	
PP LDO5 FILT	FUNC_TEST=TRUE 59
SIMCRD RST CONN FILT	FUNC_TEST=TRUE 59 71
SIMCRD CLK CONN FILT	FUNC_TEST=TRUE 59 71
SIMCRD IO CONN FILT	FUNC_TEST=TRUE 59 71
SIMCRD DETECT FILT	FUNC_TEST=TRUE 59 71

WIFI/BT	
PP PMU2BT REG ON	FUNC_TEST=TRUE 57 62 68 70
GPIO PMU2WLAN REG ON	FUNC_TEST=TRUE 57 62 68 70
CLK PMU2WLAN 32K	FUNC_TEST=TRUE 57 62 68 70

CAMERA - REAR	
ISP CAM REAR CLK F	FUNC_TEST=TRUE 20 21
ISP CAM REAR SCL F	FUNC_TEST=TRUE 20 21
ISP CAM REAR SDA F	FUNC_TEST=TRUE 20 21
ISP CAM REAR SHUTDOWN L F	FUNC_TEST=TRUE 20 21

CAMERA - FRONT	
ISP CAM FRONT CLK F	FUNC_TEST=TRUE 20 21
ISP CAM FRONT SCL F	FUNC_TEST=TRUE 20 21
ISP CAM FRONT SDA F	FUNC_TEST=TRUE 20 21
ISP CAM FRONT SHUTDOWN L F	FUNC_TEST=TRUE 20 21

MESA	
GPIO MESA2SOC IRO FILT	FUNC_TEST=TRUE 31 33
MESA BOOST ENABLE FILT	FUNC_TEST=TRUE 31 33
SPI MESA MISO FILT	FUNC_TEST=TRUE 31 33
SPI MESA MOSI FILT	FUNC_TEST=TRUE 31 33
SPI MESA SCLK FILT	FUNC_TEST=TRUE 31 33

HALL EFFECT	
GPIO HALL2PMU IRO0	FUNC_TEST=TRUE 19 62
GPIO HALL2PMU IRO1 FILT	FUNC_TEST=TRUE 29 30
PP3V0 S2R GRAPE HALL FILT	FUNC_TEST=TRUE 29 30

ALS	
PP3V0 MIC ALS FILT	FUNC_TEST=TRUE 23
PP3V0 HP ALS FILT	FUNC_TEST=TRUE 23
GPIO HP ALS2SOC IRO L FILT	FUNC_TEST=TRUE 23
GPIO MIC ALS2SOC IRO L F	FUNC_TEST=TRUE 23

I2C HP ALS SCL 1V8 FILT	
I2C HP ALS SDA 1V8 FILT	FUNC_TEST=TRUE 23 70
I2C MIC ALS SCL 1V8 F	FUNC_TEST=TRUE 23 70
I2C MIC ALS SDA 1V8 F	FUNC_TEST=TRUE 23 70

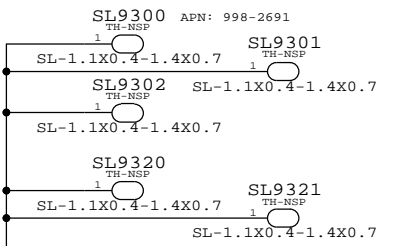
DISPLAY	
EDP HPD EMI	FUNC_TEST=TRUE 32

OSCAR	
CLK PMU2OSCAR 32K AND RESET L	FUNC_TEST=TRUE 17 62 70

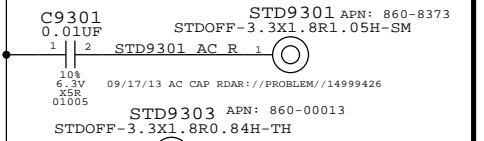
SOCHOT0 L	
	FUNC_TEST=TRUE 6 62

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

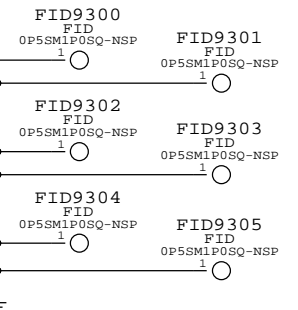
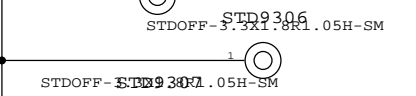


FOREHEAD B2B STANDOFFS
STD9300 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM



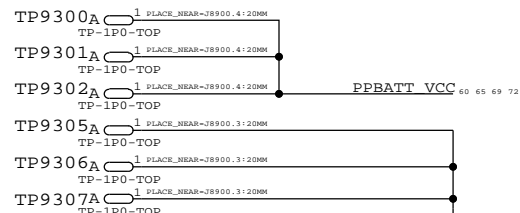
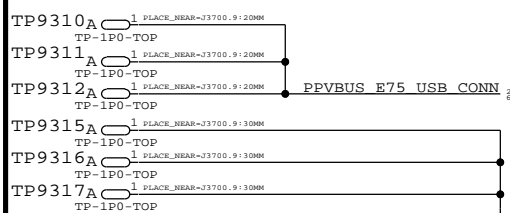
BUTTON FLEX B2B STANDOFFS
STD9302 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM

GRAPE AND DISPLAY B2B STANDOFFS
STD9305 APN: 860-8373
STDOFF-3.3X1.8R1.05H-SM



DEV BOARD NET TERMINATION

NC SOC GPIO09	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO ALS2SOC DEVBRD IRO L	6
NC PMU GPIO20	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO DEVBRD2PMU WAKE L	62
NC ULPI STP	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO SOC2DEVBRD S3E WAKE	6
NC ULPI DATA3	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO SOC2DEVBRD S3E RESET2 L	6
NC PCIE CLKREQ2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE DEVBRD2SOC CLKREQ L	6
NC PCIE PERST2	NO_TEST=TRUE MAKE_BASE=TRUE	PCIE SOC2DEVBRD RESET L	6
NC NAND SYS CLK	NO_TEST=TRUE MAKE_BASE=TRUE	CLK SOC2DEVBRD PCIE 24MHZ	6
NC I2S4 MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO DISPLAY ID0	6
NC I2S1 MCK	NO_TEST=TRUE MAKE_BASE=TRUE	GPIO DISPLAY ID1	6



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE		TEST: TPS/HOLES/FIDUCUALS	
Apple Inc.		DRAWING NUMBER	051-0301
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EE CHARACTERIZATION TP

SOC

PP9501	1	RESET SOC L	PLACE_SIDE=TOP	4 5 10 25 62 68 69
PP9503	1	SOCHOT0 L R		62
PP9502	1	TP ANALOGMUXOUT		5

PP9507	1	PPVDD CPU SOC SENSE	PLACE_NEAR=U0600_A031:1.5MM	13 62
PP9508	1	PPVDD GPU SOC SENSE	PLACE_NEAR=U0600_N261:1.5MM	13 62
PP9588	1	PPVDD SRAM SOC SENSE	PLACE_NEAR=U0600_N251:1.5MM	13 62
PP9513	1	PPVDD SOC SOC SENSE	PLACE_NEAR=U0600_N25:1.5MM	13 62

PP9509	1	TP SOC VSS SENSE	PLACE_NEAR=U0600_M26:1.5MM	12
PP9510	1	TP SOC VSS CPU SENSE	PLACE_NEAR=U0600_A03:1.5MM	12

ANCO AD<1..7>	FUNC_TEST=TRUE	7 16
ANCO CR0 L	FUNC_TEST=TRUE	7 16 69
ANCO ALE	FUNC_TEST=TRUE	7 16
ANCO CLE	FUNC_TEST=TRUE	7 16
ANCO WE L	FUNC_TEST=TRUE	7 16
ANCO RE L	FUNC_TEST=TRUE	7 16

ANC1 AD<0>	FUNC_TEST=TRUE	7 16
ANC1 CR0 L	FUNC_TEST=TRUE	7 16 69
ANC1 ALE	FUNC_TEST=TRUE	7 16
ANC1 CLE	FUNC_TEST=TRUE	7 16
ANC1 WE L	FUNC_TEST=TRUE	7 16
ANC1 RE L	FUNC_TEST=TRUE	7 16
ANC1 DOS	FUNC_TEST=TRUE	7 16

PPVREF ANC SOC	FUNC_TEST=TRUE	7
PPVREF ANC NAND	FUNC_TEST=TRUE	7
NAND SLOTO RDYBSY L	FUNC_TEST=TRUE	16

PP9505	1	ANC0 AD<0>	PLACE_SIDE=BOTTOM	7 16
PP9506	1	ANC0 DOS	PLACE_SIDE=BOTTOM	7 16
PP9500	1	GND	(PLACE_SIDE=TOP)	16
PP9504	1	=PP1V8 NAND	(PLACE_SIDE=TOP)	16 72
PP9509	1	TP ANC TCKC NAND	(PLACE_SIDE=TOP)	16
PP9504	1	TP ANC TMSC NAND	(PLACE_SIDE=TOP)	16

PMU

GPIO PMU2BBPMU RESET L	FUNC_TEST=TRUE	62 68 69 71
GPIO BT2PMU HOST WAKE	FUNC_TEST=TRUE	57 62 68 70
GPIO BB2PMU HOST WAKE L	FUNC_TEST=TRUE	62 68 69
GPIO CODEC2PMU HS IRO L	FUNC_TEST=TRUE	62 68 69
PMU TCAL	FUNC_TEST=TRUE	62
CLK PMU2WLAN 32K	FUNC_TEST=TRUE	57 62 68 69 70
CLK PMU2OSCAR 32K AND RESET	FUNC_TEST=TRUE	17 62 69
PA NTC P	FUNC_TEST=TRUE	62 68
BOARD TEMP2 P	FUNC_TEST=TRUE	62
BOARD TEMP3 P	FUNC_TEST=TRUE	62
BOARD TEMP4 P	FUNC_TEST=TRUE	62
BOARD TEMP5 P	FUNC_TEST=TRUE	62
BOARD TEMP6 P	FUNC_TEST=TRUE	62
BOARD TEMP7 P	FUNC_TEST=TRUE	62
BOARD TEMP8 P	FUNC_TEST=TRUE	62
TP BUCK LDO UOV	FUNC_TEST=TRUE	62
TP BUCK SLDP MUX	FUNC_TEST=TRUE	62
TP AMUX AY	FUNC_TEST=TRUE	62
TP AMUX BY	FUNC_TEST=TRUE	62

PP9511	1	DWI SOC2PMU CLK	NO_TEST=TRUE	6 62
PP9512	1	DWI SOC2PMU DO	NO_TEST=TRUE	6 62
PP95F1	1	SYS ALIVE		62

GRAPE

I2C GRAPE SDA 1V8	(CUMULUS TDO) FUNC_TEST=TRUE	29 30
TP JTAG CUMULUS M TCK	FUNC_TEST=TRUE	70
TP JTAG CUMULUS M TDI	FUNC_TEST=TRUE	30
JTAG CUMULUS M TMS	FUNC_TEST=TRUE	30
SPI GRAPE SCLK	FUNC_TEST=TRUE	6 30
SPI GRAPE MISO	FUNC_TEST=TRUE	6 30
SPI GRAPE MOSI	FUNC_TEST=TRUE	6 30
SPI GRAPE CS L	FUNC_TEST=TRUE	6 30
GPIO SOC2GRAPE RESET L	FUNC_TEST=TRUE	6 30
GPIO GRAPE2SOC IRO L	FUNC_TEST=TRUE	6 30
DISPLAY SYNC	FUNC_TEST=TRUE	6 30
CLK SOC2GRAPE 32K	FUNC_TEST=TRUE	9 30 69
CUMULUS M2S CLK	FUNC_TEST=TRUE	30
CUMULUS M2S SDA	FUNC_TEST=TRUE	30
I2C GRAPE SDA 1V8	FUNC_TEST=TRUE	29 30 70
I2C GRAPE SCL 1V8	FUNC_TEST=TRUE	29 30

PP9514	1	TP CUMULUS S CS L		30
PP9515	1	TP CUMULUS S GPIO 3		30

AUDIO

DMIC MIC SD	FUNC_TEST=TRUE	22 23
DMIC BTN SD	FUNC_TEST=TRUE	22 23
GPIO CODEC2SOC IRO L	FUNC_TEST=TRUE	6 22

TP9500A	1	TP-P5		
TP9501A	1	SPKRAMP R OUT P	FUNC_TEST=TRUE	24 27 69
TP9502A	1	SPKRAMP R OUT N	FUNC_TEST=TRUE	24 27 69
TP9503A	1	ATP-P5		
TP9510A	1	ATP-P5		
TP9511A	1	SPKRAMP L OUT P	FUNC_TEST=TRUE	24 27 69
TP9512A	1	SPKRAMP L OUT N	FUNC_TEST=TRUE	24 27 69
TP9513A	1	P5		

PP95D0	1	I2S SOC2SPKRAMP MCK		6 24
PP95D1	1	I2S SOC2SPKRAMP BCLK		6 24
PP95D2	1	I2S SOC2SPKRAMP LRCK		6 24
PP95D3	1	I2S SOC2SPKRAMP DOUT		6 24
PP95D4	1	I2S SPKRAMP2SOC DOUT		6 24
PP95D7	1	I2S SOC2CODEC ASP MCK		6 22
PP95D8	1	I2S SOC2CODEC ASP BCLK		6 22
PP95D9	1	I2S SOC2CODEC ASP LRCK		6 22
PP95DA	1	I2S SOC2CODEC ASP DOUT		6 22
PP95DB	1	I2S CODEC2SOC ASP DOUT		6 22
PP95DC	1	I2S SOC2CODEC XSP BCLK		6 22
PP95DD	1	I2S SOC2CODEC XSP LRCK		6 22
PP95DE	1	I2S SOC2CODEC XSP DOUT		6 22
PP95DF	1	I2S CODEC2SOC XSP DOUT		6 22

CAMERA - FRONT				
PP9520	1	MIPI CAM FRONT CLK P	PLACE_NEAR=U0600_A036:1.5MM	8 21 70
PP9521	1	MIPI CAM FRONT CLK N	PLACE_NEAR=U0600_A036:1.5MM	8 21 70
PP9522	1	MIPI CAM FRONT DATA P<0>	PLACE_NEAR=U0600_A037:1.5MM	8 21 70
PP9523	1	MIPI CAM FRONT DATA N<0>	PLACE_NEAR=U0600_A037:1.5MM	8 21 70
CAMERA - REAR				
PP9524	1	MIPI CAM REAR CLK P	PLACE_NEAR=U0600_A031:1.5MM	8 21 70
PP9525	1	MIPI CAM REAR CLK N	PLACE_NEAR=U0600_A031:1.5MM	8 21 70
PP9526	1	MIPI CAM REAR DATA P<0>	PLACE_NEAR=U0600_A031:1.5MM	8 21 70
PP9527	1	MIPI CAM REAR DATA N<0>	PLACE_NEAR=U0600_A031:1.5MM	8 21 70

OSCAR

PP95C0	1	TP OSCAR P0 05		17
PP95C1	1	TP OSCAR P0 06		17
PP95C2	1	TP OSCAR P0 09		17
PP95C3	1	TP OSCAR P0 17		17
PP95C4	1	TP OSCAR P0 21		17
PP95C8	1	TP OSCAR P1 02		17
PP95C9	1	TP OSCAR P1 03		17
PP95CD	1	SWD_OSCAR_I0_1V8		9 17
PP95CE	1	SWD_OSCAR_CLK_1V8		9 17

CHAN 0 NEAR DRAM				
PP9534	1	DDR0 CK P	PLACE_NEAR=U1600_W13:1MM	10 15 70
PP9535	1	DDR0 CK N	PLACE_NEAR=U1600_W13:1MM	10 15 70
PP9536	1	DDR0 CKE<0>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9537	1	DDR0 CA<0>	PLACE_NEAR=U1600_W17:1MM	10 15 70
PP9538	1	DDR0 CA<1>	PLACE_NEAR=U1600_W17:1MM	10 15 70
PP9539	1	DDR0 CA<2>	PLACE_NEAR=U1600_W16:1MM	10 15 70
PP9540	1	DDR0 CA<3>	PLACE_NEAR=U1600_W16:1MM	10 15 70
PP9541	1	DDR0 CSN<0>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9542	1	DDR0 CSN<1>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9543	1	DDR0 CSN<2>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9544	1	DDR0 CSN<3>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9545	1	DDR0 DOS P<0>	PLACE_NEAR=U1600_W15:1MM	10 15 70
PP9546	1	DDR0 DOS N<0>	PLACE_NEAR=U1600_W14:1MM	10 15 70
PP9547	1	DDR0 DQ<0>	PLACE_NEAR=U1600_C17:1MM	10 15 70

CHAN 0 NEAR SOC				
PP9570	1	DDR0 DOS P<0>	PLACE_NEAR=U0600_D7:1MM	10 15 70
PP9571	1	DDR0 DOS N<0>	PLACE_NEAR=U0600_D6:1MM	10 15 70
PP9572	1	DDR0 DQ<0>	PLACE_NEAR=U0600_P10:1MM	10 15 70

CHAN 1 NEAR DRAM				
PP9542	1	DDR1 DOS P<0>	PLACE_NEAR=U1600_K4:1MM	10 15 70
PP9543	1	DDR1 DOS N<0>	PLACE_NEAR=U1600_K4:1MM	10 15 70
PP9544	1	DDR1 DQ<0>	PLACE_NEAR=U1600_K3:1MM	10 15 70

CHAN 1 NEAR SOC				
PP9572	1	DDR1 DOS P<0>	PLACE_NEAR=U0600_V1:1MM	10 15 70
PP9573	1	DDR1 DOS N<0>	PLACE_NEAR=U0600_U1:1MM	10 15 70
PP9574	1	DDR1 DQ<0>	PLACE_NEAR=U0600_AA3:1MM	10 15 70

WIFI

TP JTAG WLAN TMS	FUNC_TEST=TRUE	68
JTAG WLAN SEL TRST	(TD1) FUNC_TEST=TRUE	68
JTAG WLAN SEL TRST	(TD0) FUNC_TEST=TRUE	6 57 68
WLAN SOC2WLAN RTS L	FUNC_TEST=TRUE	57
OSCAR2RADIO CONTEXT A	FUNC_TEST=TRUE	57 68
FUNC_TEST=TRUE		57 68
SOC2BT	FUNC_TEST=TRUE	6 57 68
TRU	FUNC_TEST=TRUE	6 57 68
UART_SOC2WLAN_TX	WLAN2SOC	6 57 71
UART_WLAN2BB_COEX_TX	FUNC_TEST=TRUE	40 57 71
I2S SOC2BT LRCK	FUNC_TEST=TRUE	57 68
I2S BT2SOC DOUT	FUNC_TEST=TRUE	6 57 68
CLK_PMU2WLAN_32K	FUNC_TEST=TRUE	57 62 68 69 70
GPIO PMU2WLAN REG ON	FUNC_TEST=TRUE	57 62 68 69
GPIO2PMU2WLANWAKE	FUNC_TEST=TRUE	57 62
GPIO2PMU2WLANWAKE	FUNC_TEST=TRUE	57 62
GPIO2PMU2WLANWAKE	FUNC_TEST=TRUE	57 62
GPIO2PMU2WLANWAKE	FUNC_TEST=TRUE	57 62

OTHER PPS				
PP95B8	1	WLAN GPIO 8	NO_TEST=TRUE	57
PP95B9	1	WLAN GPIO 10	NO_TEST=TRUE	57

I2C

I2C OSCAR2PROX SDA 1V8	FUNC_TEST=TRUE	17 58
I2C OSCAR2PROX SCL 1V8	FUNC_TEST=TRUE	17 58
I2C0 SCL 1V8	FUNC_TEST=TRUE	6
I2C0 SDA 1V8	FUNC_TEST=TRUE	6
I2C1 SCL 1V8	FUNC_TEST=TRUE	6
I2C1 SDA 1V8	FUNC_TEST=TRUE	6
I2C2 SCL 1V8	FUNC_TEST=TRUE	6
I2C2 SDA 1V8	FUNC_TEST=TRUE	6

PP95F4	1	=I2C3 SDA 1V8		4
PP95F5	1	=I2C3 SCL 1V8		4

I2C HP ALS SDA 1V8 FILT	FUNC_TEST=TRUE	23 69
I2C HP ALS SDA 1V8 FILT	FUNC_TEST=TRUE	23 69
I2C MIC ALS SCL 1V8 F	FUNC_TEST=TRUE	23 69
I2C MIC ALS SDA 1V8 F	FUNC_TEST=TRUE	23 69

UART

UART SOC2ACC TX	FUNC_TEST=TRUE	6 25
UART ACC2SOC TX	FUNC_TEST=TRUE	6 25
UART SOC2OSCAR TX	FUNC_TEST=TRUE	6 17
UART OSCAR2SOC TX	FUNC_TEST=TRUE	6 17

CHAN 2 NEAR DRAM				
PP9548	1	DDR2 CK P	PLACE_NEAR=U1700_W13:1MM	10 15 70
PP9549	1	DDR2 CK N	PLACE_NEAR=U1700_W13:1MM	10 15 70
PP9550	1	DDR2 CKE<0>	PLACE_NEAR=U1700_W14:1MM	10 15 70
PP9551	1	DDR2 CA<0>	PLACE_NEAR=U1700_W17:1MM	10 15 70
PP9552	1	DDR2 CA<1>	PLACE_NEAR=U1700_W17:1MM	10 15 70
PP9553	1	DDR2 CA<2>	PLACE_NEAR=U1700_W16:1MM	10 15 70
PP9554	1	DDR2 CA<3>	PLACE_NEAR=U1700_W16:1MM	10 15 70
PP9555	1	DDR2 CSN<0>	PLACE_NEAR=U1700_W14:1MM	10 15 70
PP9556	1	DDR2 CSN<1>	PLACE_NEAR=U1700_W14:1MM	10 15 70
PP9557	1	DDR2 CSN<2>	PLACE_NEAR=U1700_W14:1MM	10 15 70
PP9558	1	DDR2 CSN<3>	PLACE_NEAR=U1700_W14:1MM	10 15 70
PP9559	1	DDR2 DOS P<0>	PLACE_NEAR=U1700_D15:1MM	10 15 70
PP9560	1	DDR2 DOS N<0>	PLACE_NEAR=U1700_D14:1MM	10 15 70
PP9561	1	DDR2 DQ<0>	PLACE_NEAR=U1700_C17:1MM	10 15 70

CHAN 2 NEAR SOC				
PP9585	1	DDR2 DOS P<0>	PLACE_NEAR=U0600_A01:1MM	10 15 70
PP9586	1	DDR2 DOS N<0>	PLACE_NEAR=U0600_A01:1MM	10 15 70
PP9587	1	DDR2 DQ<0>	PLACE_NEAR=U0600_A03:1MM	10 15 70

CHAN 3 NEAR DRAM				
PP9556	1	DDR3 DOS P<0>	PLACE_NEAR=U1700_K4:1MM	10 15 70
PP9557	1	DDR3 DOS N<0>	PLACE_NEAR=U1700_L4:1MM	10 15 70
PP9558	1	DDR3 DQ<0>	PLACE_NEAR=U1700_K3:1MM	10 15 70

CHAN 3 NEAR SOC				
PP9596	1	DDR3 DOS P<0>	PLACE_NEAR=U0600_A010:1MM	10 15 70
PP9597	1	DDR3 DOS N<0>	PLACE_NEAR=U0600_A011:1MM	10 15 70
PP9598	1	DDR3 DQ<0>	PLACE_NEAR=U0600_A07:1MM	10 15 70

CHAN 3 NEAR SOC				
PP9596	1	DDR3 DOS P<0>	PLACE_NEAR=U0600_A010:1MM	10 15 70
PP9597	1	DDR3 DOS N<0>	PLACE_NEAR=U0600_A011:1MM	10 15 70
PP9598	1	DDR3 DQ<0>	PLACE_NEAR=U0600_A07:1MM	10 15 70

PP95B5	1	UART WLAN2SOC RTS L		6 68
PP95B6	1	UART BT2SOC RTS L		6 68
PP95B7	1	UART SOC2BT RTS L		6 57 68

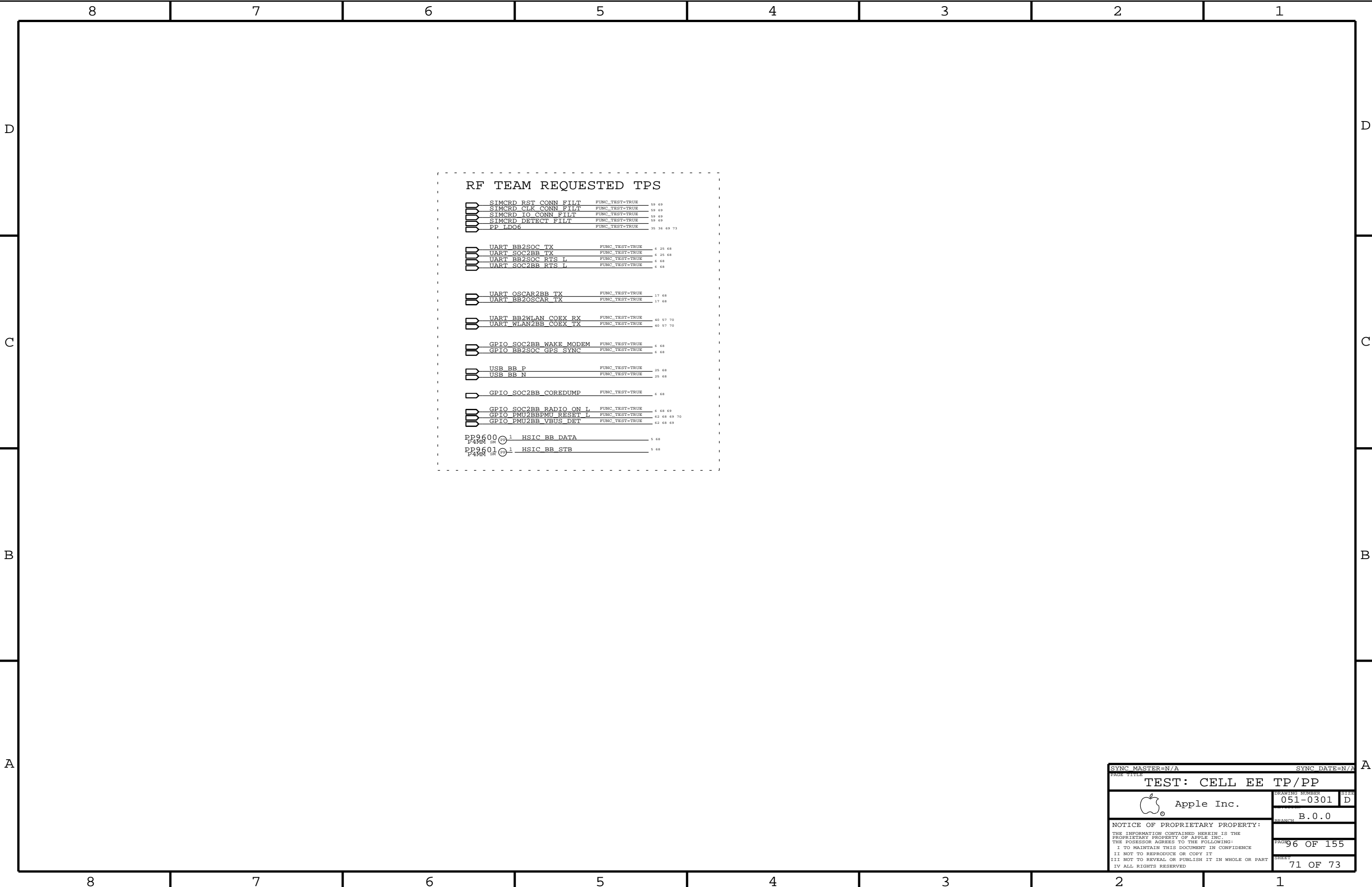
SOC SIDE PCIE TPS				
PP95A0	1	PLACE_NEAR=U0600_D28:1MM	PCIE_WLAN2SOC_TX_P	9 68 70
PP95A1	1	PLACE_NEAR=U0600_D28:1MM	PCIE_WLAN2SOC_TX_N	9 68 70

REMOVED PCIE SOC2WLAN TX C P PP BECAUSE THE IT BLOCKED THE SHIM RING.				
REMOVED PCIE SOC2WLAN TX C N PP BECAUSE THE P VERSION WAS REMOVED				
PP95A6	1	PLACE_NEAR=U0600_J40:1MM	PCIE_WLAN2SOC_CLKREQ_L	9 68 70

WLAN SIDE PCIE TPS				
PP95A7	1	PLACE_NEAR=U07500_731:1MM	PCIE_WLAN2SOC_TX_C_P	9 68 70
PP95A8	1	PLACE_NEAR=U07500_74:1MM	PCIE_WLAN2SOC_TX_C_N	9 57 68 70
PP95A9	1	PLACE_NEAR=U07500_76:1MM	PCIE SOC2WLAN_TX_P	9 57 68 70
PP95B0	1	PLACE_NEAR=U07500_76:1MM	PCIE SOC2WLAN_TX_N	9 57 68 70
PP95B1	1	PLACE_NEAR=U07500_71:1MM	PCIE SOC2WLAN_CLK_P	9 68 70
PP95B2	1	PLACE_NEAR=U07500_70:1MM	PCIE SOC2WLAN_CLK_N	9 68 70
PP95B3	1	PLACE_NEAR=U07500_1:1MM	PCIE SOC2WLAN_RESET_L	9 68 70

HIGH SPEED, NO TEST

DDR0 CA<0..9>	NO_TEST=TRUE	10 14 70
DDR0 CK P	NO_TEST=TRUE	10 14 70
DDR0 CK N	NO_TEST=TRUE	10 14 70
DDR0 CKE<0..9>	NO_TEST=TRUE	10 14 70
DDR0 CSN<0..1>	NO_TEST=TRUE	10 14 70
DDR0 CSN<0..1>	NO_TEST=TRUE	10 14 70
DDR0 DM<0..3>	NO_TEST=TRUE	10 14 70
DDR0 DOS<0..31>	NO_TEST=TRUE	10 14 70
DDR0 DOS P<0..3>	NO_TEST=TRUE	10 14 70
DDR0 DOS N<0..3>	NO_TEST=TRUE	10 14 70
DDR1 CA<0..9>	NO_TEST=TRUE	10 14 70
DDR1 CK P	NO_TEST=TRUE	10 14 70
DDR1 CK N	NO_TEST=TRUE	10 14 70
DDR1 CA<0..9>	NO_TEST=TRUE	10 14 70
DDR1 CKE<0..1>	NO_TEST=TRUE	10 14 70
DDR1 CSN<0..1>	NO_TEST=TRUE	10 14 70
DDR1 DM<0..3>	NO_TEST=TRUE	10 14 70
DDR1 DOS<0..31>	NO_TEST=TRUE	10 14 70
DDR1 DOS P<0..3>	NO_TEST=TRUE	10 14 70
DDR1 DOS N<0..3>	NO_TEST=TRUE	10 14 70
DDR2 CA<0..9>	NO_TEST=TRUE	10 15 70
DDR2 CK P	NO_TEST=TRUE	10 15 70
DDR2 CK N	NO_TEST=TRUE	10 15 70
DDR2 CA<0..9>	NO_TEST=TRUE	10 15 70
DDR2 CKE<0..1>	NO_TEST=TRUE	10 15 70
DDR2 CSN<0..1>	NO_TEST=TRUE	10 15 70
DDR2 DM<0..3>	NO_TEST=TRUE	10 15 70
DDR2 DOS<0..31>	NO_TEST=TRUE	10 15 70
DDR2 DOS P<0..3>	NO_TEST=TRUE	10 15 70
DDR2 DOS N<0..3>	NO_TEST=TRUE	10 15 70
DDR3 CA<0..9>	NO_TEST=TRUE	10 15 70
DDR3 CK P	NO_TEST=TRUE	10 15 70
DDR3 CK N	NO_TEST=TRUE	10 15 70
DDR3 CA<0..9>	NO_TEST=TRUE	10 15 70
DDR3 CKE<0..1>	NO_TEST=TRUE	10 15 70
DDR3 CSN<0..1>	NO_TEST=TRUE	10 15 70
DDR3 DM<0..3>	NO_TEST=TRUE	10 15 70
DDR3 DOS<0..31>	NO_TEST=TRUE	10 15 70
DDR3 DOS P<0..3>	NO_TEST=TRUE	10 15 70
DDR3 DOS N<0..3>	NO_TEST=TRUE	10 15 70



POWER CONNECTIONS

BUCK0 (DWI DVC)

69 60 PPVDD CPU == =PPVDD CPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK1 (DWI DVC)

69 60 PPVDD GPU == =PPVDD GPU 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK2

69 60 PP0V95 SOC == =PP0V95 SOC 12
MAKE_BASE=TRUE
VOLTAGE=0.95V
== =PP0V95 PCIE SOC 9
== =PP0V95 USB SOC 5

BUCK3

69 61 60 PP1V8 S2R == =PP1V8 S2R DDR 14 15
MAKE_BASE=TRUE
VOLTAGE=1.8V
== =PP1V8 S2R GRAPE EXTERNAL SW 30
== =PP1V8 S2R TRISTAR 25
== =PP1V8 S2R VDDIO WLAN BT 68
== =PP1V8 S2R MISC 6 9 66 67
== =PP1V8 S2R EXTERNAL SW 64
== =PP1V8 S2R ROTTERDAM 34

BUCK3_SW

BUCK3_SW1

69 67 60 PP1V8 SW1 == =PP1V8 AUDIO 22 24
MAKE_BASE=TRUE
VOLTAGE=1.8V
== =PP1V8 SW1 EXT SW ON 64
XWC130 SW
1 2 PP1V8 SW1 FOREHEAD 69 72
69 69 PP1V8 SW1 FOREHEAD == =PP1V8 CAM FRONT 21
MAKE_BASE=TRUE
VOLTAGE=1.8V
== =PP1V8 CAM REAR 21
== =PP1V8 DMIC 23 28

BUCK3_SW1_EXT

69 64 PP1V8 EXT SW == =PP1V8 VDDIO18 SOC 11
MAKE_BASE=TRUE
VOLTAGE=1.8V
== =PP1V8 XTAL SOC 11
== =PP1V8 PCIE SOC 9
== =PP1V8 MIPI SOC 8
== =PP1V8 NAND SOC 7
== =PP1V8 NAND 16 70
== =PP1V8 NAND EXT SW ON 64
== =PP1V8 SOC 4 5 6 62
== =PP1V8 EEPROM 6

BUCK3_SW2

69 60 PP1V8 SW2 == =PP1V8 SPKRAMP DVDD 24
MAKE_BASE=TRUE
VOLTAGE=1.8V
69 30 PP1V8 GRAPE EXT SW == =PP1V8 GRAPE EXT SW 29 30
MAKE_BASE=TRUE
VOLTAGE=1.8V

BUCK3_SW3

69 60 PP1V8 S2R SW3 == =PP1V8 S2R OSCAR 17
MAKE_BASE=TRUE
VOLTAGE=1.8V
== =PP1V8 S2R PHOS 18
== =PP1V8 S2R GYRO 18
== =PP1V8 S2R COMPASS 18
== =PP1V8 S2R ACCEL 18
== =PP1V8 S2R PROX 58

BUCK4

69 61 60 PP1V2 S2R == =PP1V2 EXTERNAL SW 64
MAKE_BASE=TRUE
VOLTAGE=1.2V
== =PP1V2 S2R DDR 14 15
== =PP1V2 S2R DDR SOC 10

BUCK4_SW1

69 60 PP1V2 SW1 == =PP1V2 EXT SW ON 64
MAKE_BASE=TRUE
VOLTAGE=1.2V
69 64 PP1V2 EXT SW == =PP1V2 DDR VDDQ 14 15
MAKE_BASE=TRUE
VOLTAGE=1.2V
== =PP1V2 VDDIOD SOC 10 11
== =PP1V2 HSIC SOC 5
== =PP1V2 PLL SOC 9 11
== =PP1V2 CAM FRONT 21

BUCK4_SW2

69 60 PP1V2 S2R SW2 == =PP1V2 S2R OSCAR 17
MAKE_BASE=TRUE
VOLTAGE=1.2V

BUCK5 (DWI DVC)

69 60 PPVDD SRAM == =PPVDD SRAM 13
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK6

69 60 PP3V3 S2R == =PP3V3 S2R EXTERNAL SW 64
MAKE_BASE=TRUE
VOLTAGE=3.3V
== =PP3V3 S2R WIFI PA 68
69 64 PP3V3 EXT SW == =PP3V3 NAND 16
MAKE_BASE=TRUE
VOLTAGE=3.3V
== =PP3V3 USB SOC 5

LDO1

69 61 PP3V0 S2R HALL == =PP3V0 S2R HALL 19 30
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO2

69 61 PP1V7 VA VCP == =PP1V7 VA VCP 22
MAKE_BASE=TRUE
VOLTAGE=1.7V

LDO3

69 61 PP3V0 S2R SENSOR == =PP3V0 S2R PROX 58
MAKE_BASE=TRUE
VOLTAGE=3.0V
== =PP3V0 S2R COMPASS 18
== =PP3V0 S2R GYRO 18

LDO4

69 61 PP3V0 ALS == =PP3V0 HP ALS 23
MAKE_BASE=TRUE
VOLTAGE=3.0V
== =PP3V0 MIC ALS 23

LDO5

69 61 PP3V1 S2R MESA == =PP3V1 S2R MESA 33
MAKE_BASE=TRUE
VOLTAGE=3.1V

LDO6

69 61 PP3V3 ACC == =PP3V3 ACC 25
MAKE_BASE=TRUE
VOLTAGE=3.3V

LDO7

69 61 PP3V0 S2R TRISTAR == =PP3V0 S2R TRISTAR 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
== =PP3V0 S2R ANT SW 59

LDO8

72 69 61 PP3V0 MISC == PP3V0 MISC 61 69 72
MAKE_BASE=TRUE
VOLTAGE=3.0V

LDO9

69 61 PP1V25 CAM == =PP1V25 CAM REAR 21
MAKE_BASE=TRUE
VOLTAGE=1.25V

LDO10

69 61 PP1V0 SOC == =PP1V0 MIPI SOC 8
MAKE_BASE=TRUE
VOLTAGE=1.0V
== =PP1V0 LPDP SOC 9

LDO11

69 61 PP2V6 CAM AF == =PP2V6 CAM REAR AF 21
MAKE_BASE=TRUE
VOLTAGE=2.6V

LDO13

69 61 PP2V9 CAM == =PP2V9 CAM FRONT 21
MAKE_BASE=TRUE
VOLTAGE=2.9V
== =PP2V9 CAM REAR 21

LDO14

72 69 61 PP1V8 SPARE == PP1V8 SPARE 61 69 72
MAKE_BASE=TRUE
VOLTAGE=1.8V

VLCM1

69 61 PP5V25 GRAPE == =PP5V25 GRAPE 29 30
MAKE_BASE=TRUE
VOLTAGE=5.25V

CHARGER MAIN

69 65 64 61 60 PPVCC MAIN == =PPVCC MAIN AUDIO 22
MAKE_BASE=TRUE
VOLTAGE=4.7V
== =PPVCC MAIN LED 63
== =PPVCC MAIN CPU 60
== =PPVCC MAIN GPU 60
== =PPVCC MAIN SOC 60
== =PPVCC MAIN GRAPE 29 30
== =PPVCC MAIN LCD 32
== =PPVCC MAIN VDD LCM 61
== =PPVCC MAIN WLAN 68
== =PPVCC MAIN MESA 13
== =PPVCC MAIN ROTTERDAM 34

BATTERY

69 65 60 PPBATT VCC == =PPBATT POS CONN 66
MAKE_BASE=TRUE
VOLTAGE=4.7V
== =PPBATT VCC_BB 68
== =PPBATT AUDIO 24

USB POWER INPUT

69 65 PPVBUS USB DCIN == =PPVBUS USB EMI 26
MAKE_BASE=TRUE
VOLTAGE=1.6V


ON_BUF

69 61 PP1V8 ALWAYS == =PP1V8 ALWAYS 4 11 62
MAKE_BASE=TRUE
VOLTAGE=1.8V

BACKLIGHT BOOST

69 61 PPLED OUT A == =PPLED REG A 32
MAKE_BASE=TRUE
VOLTAGE=20.4V

69 63 PPLED OUT B == =PPLED REG B 32
MAKE_BASE=TRUE
VOLTAGE=20.4V

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
POWER: ALIASES			
 Apple Inc.		DRAWING NUMBER	051-0301
		SIZE	D
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